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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP96/03407	November 21, 1996	

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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510 Rec'd PCT/PTO 20 MAY 1999

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendemnts has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [X] A change of power of attorney and/or address letter.
16. [X] Other items or information:

International Publication No. w098/22980-cover sheets
International Search Report w/references
Figs. 1-41

International Applica... PCT/JP96/03407 | U.S. Application No. | Attorney's Docket

17. [XX] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Search Report has been prepared by the EPO or JPO ..... $ 840.00	840.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $ 670.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... $ 490.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... $ 700.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	32 - 20 =	12	X$18.00	$ 216.00	
Independent claims	4 - 3 =	1	X$78.00	$ 78.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 1,134.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 1,134.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ]20 [ ]30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$1,134.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$1,134.00	
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a. [XX] A check in the amount of $1,134.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [XX] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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S P E C I F I C A T I O N

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

The present invention relates generally to semiconductor devices and manufacturing methodology thereof, and more particularly to technologies usefully applicable to high-density mountable semiconductor devices with tape carrier package (TCP) structures along with fabrication methods thereof.

BACKGROUND ART

In recent years, as portable or handheld electronic equipment less in shape and thickness and yet with much increased functionalities is developed for mass production, TCP technologies are becoming important more and more in the manufacture of solid-state integrated circuit (IC) packages for use in such highly advanced electronic equipment due to the enhanced mountability of thickness-reduced or "thin" electronics components and also the ability to increase package pins in number.

The TCP is a package structured including a tape carrier having a plurality of conductive leads formed thereon in a repeated pattern, wherein a semiconductor chip is placed on or in the tape carrier with its

electrode pads lamination-contacted with corresponding ones of the carrier leads for electrical interconnection therebetween, the semiconductor chip being sealed by a sealing resin material or the like.

Prior known TCPs are typically designed so that a semiconductor chip used is greater in thickness than the tape carrier, which would result in an increase in mount height of a multilayer tape structure with multiple unitary tape carriers laminated on one another. One prior art approach to mount-height reduction has been disclosed, for example, in Japanese Patent Application Laid-Open No. 63(1985)-52431 ("JP-A-63-52431"), which teaches a tape carrier for use with a certain semiconductor chip having its bottom or back surface cut away. Another approach is found in JP-A-5(1993)-291218, which discloses therein a technique for making thinner both the semiconductor chip and the tape carrier at a time.

Another TCP structure is also known which includes a specific frame structure, called the "stiffener" in the semiconductor device art, provided around a semiconductor chip with its back surface contacted with a heat release member known as "heat spreader." In this TCP a tape carrier is mounted on the stiffener for junction between one end of its lead

and the semiconductor chip while simultaneously providing a bump electrode at the other end of such lead. In this case the resultant TCP structure suffers from an excessive increase in thickness, which would result in incapability of achieving any intended multilayer structures.

Still another TCP structure is found through analysis activities made by the inventors named in the subject application for patent, which is designed to employ a semiconductor chip that is thinner than a tape carrier having an opening called the "device hole." The "thin" semiconductor chip is disposed in the tape carrier's device hole with its back surface being substantially at the same level as or coplanar with the bottom surface of the tape carrier. The principal surface and sidewalls of such semiconductor chip are coated with a chosen sealing resin material. Unfortunately, this prior art TCP structure is encountered with a problem which follows: The semiconductor chip can warp after completion of sealing processes due to the fact that only its principal surface and sidewalls are partly subject to sealing by use of the seal resin. To this end, the prior art must be designed to employ an extra hard or rigid plate for use in eliminating occurrence of chip

cracks in the back surface of the semiconductor chip. However, this does not come without an additional problem: The resultant TCP increases in thickness discouraging experts in the art from attempting to use such "thick" TCP to attain their intended multilayer structure. While a structure with a seal plate provided on the seal resin is known, this also suffers from the TCP thickness increase problem, which is neither suitable for use as multilayer structure. Additionally, a thin package structure using a film substrate with its lower surface coplanar with the back surface of a chip has been disclosed, for example, in JP-A-60(1985)-106153.

According to currently available technologies recognized by the inventors of the subject patent application, semiconductor chips used therein are thinner than tape carriers in most TCP structures. In cases where such TCPs are laminated on one another to form a multilayer structure, outer leads are typically machined to have the so-called "gull-wing" shape for elimination of unwanted contact of a semiconductor chip with its associated mount board, such as a printed circuit board. In addition, in case plural ones are to be mounted in the direction along the thickness of TCP, a specific parts-mount scheme must

be employed which includes the steps of pre-fabricating those TCPs with outer leads of different lengths, and, after completion of lead machining processes, rearranging the layout in a way such that those with low mount heights are located at lower levels whereas the remaining ones with higher mount levels are at upper levels. In this case however, different tape carriers are used to accomplish the intended overlap mounting with outer leads different in size from one another. This in turn calls for the use of a variety of types of tape carriers as well as various molding die tools, which would result in an increase in production cost therefor. Additionally, the TCP lamination mount technique is disclosed in JP-A-64(1989)-71162, for example.

It is therefore an object of the present invention to provide a technique for enabling manufacture of a semiconductor device with a TCP structure high in reliability.

Another object of this invention is to provide a technique for enabling fabrication of a thin small-size semiconductor device with TCP structures offering high-density mountability and enhanced reliability while reducing costs.

These and other objects, features and advantages

of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

SUMMARY OF THE INVENTION

A semiconductor device in accordance with the present invention is specifically arranged to include a semiconductor chip disposed in a device hole provided in a tape carrier with one end of a lead on said tape carrier being electrically connected to an external terminal of said semiconductor chip, wherein said semiconductor chip is less in thickness than said tape carrier, and wherein said semiconductor chip is sealed by a seal resin material letting a principal surface and a back surface of said semiconductor chip be coated therewith. Whereby, it becomes possible to reduce any possible stress that the semiconductor chip can receive from the principal surface and rear surface thereof.

Also, the semiconductor device of this invention is such that said semiconductor chip is disposed on a stress neutral plane extending parallel to the principal surface of said semiconductor chip at a position along a thickness of said tape carrier. This makes it possible to allow the semiconductor chip to

be placed at a location whereat the stress receivable from the TCP is kept minimal. Even in the event any external force is applied causing the TCP to deform as a whole, the semiconductor chip may remain minimal in receival of stress. It is also possible to suppress occurrence of warp of the overall TCP structure due to bimetal effects, which may in turn enable noticeable reduction of risks of chip cracks and/or connection failures during mounting assembly procedures of the semiconductor device.

In addition, the semiconductor device of the instant invention is such that a passage for use in seal resin injection is formed at part of said tape carrier thereby causing said device hole to be coupled to a gate of a metal mold structure used during formation of said seal resin. With such an arrangement, it is possible to successfully inject the seal resin so that resultant resin uniformly covers both the principal surface and rear surface of the semiconductor chip, which in turn makes it possible to greatly suppress formation of voids and/or traps in such seal resin used.

In addition, the semiconductor device of this invention is such that said tape carrier has an air exhaust port as formed letting the device hole of said

tape carrier be coupled to an air vent of the metal mold structure for use during formation of said seal resin. It is thus possible to suppress any residual air inside of the seal resin coating both the principal surface and rear surface of the semiconductor chip, which in turn enables significant reduction of creation of voids and/or traps within the seal resin. Accordingly, the semiconductor device may be further improved in reliability.

In addition, the semiconductor device of the invention is such that an electroplated metal layer is formed at part of a surface of said tape carrier in close proximity to said passage for seal resin injection, the part being brought into contact with seal resin during formation of said seal resin. Whereby, it is possible to reduce adhesive bondability between the seal resin and tape carrier, which in turn makes it possible to accelerate peel-off or debonding of resin from the tape carrier during separation between the TCP and sub-runner's resin to be carried out after the resin seal process.

In addition, the semiconductor device of the invention is such that said semiconductor chip has its back surface polished by a spin etching technique. This may permit reduction in thickness of the

semiconductor chip. Simultaneously, it is possible to make smoother the rear surface of the semiconductor chip thereby enabling the semiconductor chip to offer physically robust structure with enhanced resistivity to flexure/bending stresses while remaining hard-crackable.

In addition, a semiconductor device of the invention is arranged to have a multilayer package structure including a plurality of laminated tape carriers with a semiconductor chip less in thickness than each said tape carrier being disposed in a device hole of each said tape carrier, wherein one end of a lead provided to each of said plurality of laminated tape carriers is electrically connected to an external terminal of the semiconductor chip in the device hole of each said tape carrier, wherein each said semiconductor chip is coated with seal resin on both of a principal surface and a back surface thereof, and wherein each of said tape carriers laminated has a common signal transmission lead and a power supply lead each being electrically connected to corresponding ones of other carriers to be externally drawn out as a connection terminal being electrically connected to a lead of a mount board. With such an arrangement, it becomes possible to provide an

improved semiconductor device of the thickness-reduced or thinner TCP structure while increasing mountability or packaging density of semiconductor chips thereon.

In addition, the semiconductor device of the invention is arranged so that a connection hole is defined in each of said tape carriers laminated on one another thereby causing part of said lead to expose while permitting part of said lead to project into inside of said connection hole and also burying a conductive material in the connection hole letting a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected together. Whereby, it is possible to make sure that the lead is in contact with the conductive material within said connection hole, which in turn makes it possible to improve the connection reliability within such connection hole.

In addition, the semiconductor device of the invention is such that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while applying electroplating to inside of the connection hole thus letting each of a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to

corresponding ones of remaining carriers. Whereby, a conductive section is formed within the connection hole by use of currently available long-use electroplating techniques, which in turn enables the conductive section to be formed inside of the connection hole with minimized complexity.

In addition, the semiconductor device of the invention is such that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while inserting a conductive pin into the connection hole thus letting each of a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to corresponding ones of remaining carriers with one end of said conductive pin being extended from a mount surface of said multilayer package as said connection terminal. Whereby, it becomes possible to improve the mechanical strength or robustness of the multilayer TCP structure while reducing costs.

In addition, the semiconductor device of the invention is arranged to let a remaining end of a lead of each of said plurality of tape carriers laminated on one another extend from an outer periphery of each said tape carrier to provide a projected lead portion

being bent for lamination with others to thereby permit electrical connection between a common signal line of each of said plurality of tape carriers laminated and corresponding ones of other tape carriers and also between a power supply line of each said tape carrier and corresponding ones of other carriers. With the outer lead deformed in structure, it is possible to increase the mechanical strength of lead configuration while reducing complexity and costs. It is also possible to attain enhanced absorbability of thermal expansivity differences between the multilayered TCP and mount board.

In addition, the semiconductor device of the invention is arranged to prevent the bump electrode from contact with a certain external terminal of said semiconductor chip to permit modification of a connection route between said semiconductor chip and lead. Whereby, it is possible by use of tape carriers of the singular same type to flexibly accommodate any possible modifications or alterations as to connection routes for different signal transmission paths.

In addition, a semiconductor device manufacturing method in accordance with the invention is arranged to includes the steps of:

(a) defining a connection opening or hole in

said tape carrier letting part of said lead be exposed from the inside wall surface;

(b) burying conductive paste inside of said tape carrier;

(c) laminating multiple tape carriers each similar to said tape carrier on one another while causing said connection hole to remain uniform in formation position among them to thereby form a multilayer package; and

(d) applying thermal processing to the resultant multilayer package after completion of said lamination process step to thereby let conductive paste components residing inside of the connection holes of respective ones of said tape carriers become integral together. Whereby, it is possible to permit unitary packages to be contacted together without having any adhesive layer sandwiched between adjacent ones of them.

In addition, the semiconductor device of the invention includes the steps of:

(a) laminating by adhesive said unitary packages on one another to form a multilayer package;

(b) burying a conductive paste within a connection hole as defined in each tape carrier of said multilayer package; and

(c) applying thermal processing to said multilayer package. Whereby, it becomes possible to make adjacent unitary packages contacted with each other by use of an adhesive layer constituting the unitary packages, which in turn makes it possible to manufacture the intended multilayer TCP without suffering from an increase in process step number in the manufacture thereof.

In addition, the semiconductor device manufacturing method of the invention is such that external terminals of said semiconductor chip are contacted with leads by a single-point bonding technique while preventing a certain external terminal of said external terminals from contact with a specified lead. Whereby, it is possible by using tape carriers of the same type to accommodate any possible connection route modifications with increased flexibility.

In addition, a method of manufacturing a semiconductor device also incorporating the principles of the invention includes the steps of:

(a) preparing a tape carrier of a specified thickness with leads disposed around said device hole;

(b) preparing a semiconductor chip less in thickness than said semiconductor chip and having more

than one external terminal;

(c) disposing said semiconductor chip thinner than said tape carrier within the device hole of said tape carrier and then electrically connecting the external terminal of said semiconductor chip to one end of said lead; and

(d) after lamination of a plurality of tape carriers each with said external terminal electrically connected to the lead, sealing respective semiconductor chips disposed within device holes of respective tape carriers using seal resin at a time. Whereby, it becomes possible to reduce in number the process steps required in the manufacture of the multilayer TCP structure. It is also possible to increase or maximize the mechanical strength while improving the resistivity against humidity because of the fact that no gap spaces are formed between tape layers due to integral formation of seal resin for use in sealing multiple semiconductor chips together.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating in cross-section a semiconductor device in accordance with one preferred embodiment of the present invention; Fig. 2 is a plan view of the semiconductor device of Fig. 1; Fig. 3 is a sectional diagram of the semiconductor

device of Fig. 1 at a process step of seal resin fabrication; Figs. 4 through 10 illustrate in cross-section some of the major steps in the manufacture of the semiconductor device of Fig. 1; Fig. 11 depicts a cross-sectional view of a semiconductor device in accordance with another embodiment of this invention; Fig. 12 depicts in cross-section a semiconductor device in accordance with another embodiment of the invention; Fig. 13 shows in cross-section a semiconductor device in accordance with another embodiment of the invention; Fig. 14 shows a sectional view of a semiconductor device in accordance with another embodiment of the invention; Fig. 15 is a plan view of the semiconductor device of Fig. 14; Figs. 16 to 21 illustrate in cross-section some of the major steps in the manufacture of the semiconductor device of Fig. 14; Figs. 22-25 illustrate in cross-section some of the major steps in the manufacture of another semiconductor device of the invention; Fig. 26 shows a sectional view of a semiconductor device in accordance with another embodiment of the invention; Figs. 27-30 depict in cross-section some of the major steps in the manufacture of the semiconductor device of Fig. 26; Fig. 31 shows a sectional view of a semiconductor device in accordance with another embodiment of this

invention; Fig. 32 shows a sectional view of the semiconductor device of Fig. 31; Fig. 33 is a sectional view of a semiconductor device also embodying the invention; Fig. 34 is a sectional view of a semiconductor device also embodying the invention; Fig. 35 is a sectional view of a semiconductor device also embodying the invention; Fig. 36 is a sectional view of a semiconductor device also embodying the invention; Figs. 37-39 illustrate in cross-section some of the major steps in the manufacture of the semiconductor device shown in Fig. 36; Fig. 40 shows a plan view of a semiconductor device in accordance with a further embodiment of the invention; and, Fig. 41 is a diagram showing in cross-section the semiconductor device of Fig. 40 at a seal resin machining process step in the manufacture thereof.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Some preferred embodiments of the present invention will now be explained with reference to the accompanying drawings. Note that in all the drawings for use in explaining the embodiments, like reference characters are used to designate like parts or components and any duplicative explanation will be eliminated herein.

Firstly, a structure of a semiconductor device in accordance with a first embodiment of this invention will be explained in conjunction with Figs. 1 to 3. Note that Fig. 1 is a sectional view taken along line I-I of Fig. 2 whereas Fig. 3 is a sectional view at line III-III of Fig. 2 within a resin sealing metal mold structure. In Fig. 2 a solder resist and sealing resin are not illustrated for purposes of convenience in illustration only.

The semiconductor device of the first embodiment is the one that is adaptable for use with a semiconductor device as built in electronic equipment——such as computers, portable or mobile radiotelephone handsets, video cameras or the like——or integrated circuit (IC) cards or memory cards; for example, the semiconductor device is arranged to have a tape carrier package (TCP) structure which includes a semiconductor chip 2 disposed within a device hole 1a1 of a tape carrier 1, wherein the semiconductor chip 2 is sealed by a seal resin material 3 while causing electrodes of the semiconductor chip 2 to be externally drawn via bump electrodes 4 associated therewith.

The tape carrier 1 has a tape base member 1a, a plurality of leads 1c bonded by adhesive 1b to one

surface of the tape base 1a, and a solder resist 1d for use in coating those portions of such leads 1c which are exposed from the seal resin 3. A thickness of this tape carrier 1 as a whole may be represented by a total sum of thicknesses of constituent parts including the tape base 1a, which may typically be 167 micrometers (mm) or more or less although this value is variable among electronic products.

The tape base 1a is made of polyimide resin or other similar suitable materials, which measures 100 mm in thickness, by way of example. Tape base 1a has the device hole 1a1 which is of planar rectangular shape and is centrally defined therein. This device hole 1a1 is formed to have a slightly larger size than the chip size thereby allowing the semiconductor chip 2 to be received or housed therein.

Also in the tape base 1a, a passage or inlet port 1a2 for use in injecting resin is formed on the side of one shorter side of the device hole 1a1, which port 1a2 extends from the device hole 1a1 toward one shorter side of the outer periphery of tape base 1a. The resin injection port 1a2 is formed into a T-like planar shape, for example. As shown in Fig. 3, this resin injection port 1a2 is an opening for coupling between a gate 5a of a metal molding-die tool 5 and

the device hole 1a1 of the tape base 1a to thereby permit seal resin injected into the gate 5a to be introduced into the device hole 1a1 (cavity) through this port 1a2. In other words the resin injection port 1a2 functions as part of the gate during resin sealing processes. Whereby, it is possible to inject the seal resin 3 so that it uniformly covers surfaces of both the principal surface and back surface of the semiconductor chip 2, which in turn makes it possible to greatly reduce risks that voids and/or traps are formed inside of such seal resin 3. Note here that an arrow shown in Fig. 3 designates the flow-in direction of seal resin 3. Also note that the reference character "5b" denotes a runner whereas 5c indicates sub-runner of the metal mold.

In addition, an Au-electroplated copper thin-film layer (metal layer) 1a3, for example, is formed at a portion (hatched in Fig. 2) at which the seal resin makes contact during resin sealing processes in close proximity to the seal resin injection port 1a2 on the tape carrier 1. The copper thin-film layer 1a3 has been formed by patterning of a copper thin film used for fabrication of the leads 1c simultaneously during formation of such leads 1c; electro-plating process is also applied thereto simultaneously when plating the

leads 1c. The plated copper thin-film layer 1a3 is formed at a specified location facing the sub-runner 5c of the molding die 5 when the tape carrier 1 is disposed in the molding die 5.

This is done for the reason which follows. While such electroplated-portions are the portions from which residual resin components finally residing on the subrunner 5c are peeled off for removal, if no electroplating is applied to such portions, the adhesive strength or adhesivity of residual resin components on such portions with the tape carrier 1 can increase resulting in incapability of any successful peel-off removal of the tape carrier 1 from the metal mold used. In summary, according to the first illustrative embodiment, provision of the plated copper thin-film layer 1a3 may serve to reduce the adhesivity between residual resin at the subrunner 5c and the tape carrier 1, which in turn makes it possible to facilitate peeloff separation between the subrunner 5c's resin and the tape carrier 1.

The tape base 1a has its one surface on which multiple leads 1c are adhered by adhesive 1b that measures 12 μm in thickness, for example. The leads 1c are made of copper (Cu) formed to a thickness of approximately 35μm, for example. One end of each

lead 1c is projected into inside of the device hole 1a1, wherein the distal end surface of the projected portion is electroplated with gold (Au) by way of example. The distal end of each lead 1c is electrically connected via a bump electrode 2a to the semiconductor chip 2. This bump electrode 2a is made for example of Au as will be discussed later in the description. Accordingly, the bump electrode 2a and its associated lead 1c are in contact with each other by Au-Au junction or the like. Note that the bump electrode 2a is formed at the individual one of a plurality of bonding pads 2b disposed on the principal surface of the semiconductor chip 2 as will be discussed later, through which bump the intended electrical connection is made with respect to semiconductor integrated circuitry on the semiconductor chip 2.

In addition, a bump undercoat-layer pattern 1c1 is formed at a portion located midway between the projection end of lead 1c and the other end, which is adhered to the tape base 1a. The bump underlayer pattern 1c1 is formed so that it is greater in width than the normal region of lead 1c with the above-noted bump electrode 4 being contacted with the upper surface thereof. More specifically, an electrode of

the semiconductor chip 2 is electrically connected via the lead 1c to the bump electrode 4, and is extended toward the outside via this bump electrode 4. And, this semiconductor device is mounted for assembly on a mount substrate—such as a printed circuit board including so-called mother board—with the bump electrode 4 laid therebetween for electrical connection with the mount board's leads. Additionally, the bump electrode 4 is made for example of plumbum (Pb)-stannum (Sn) alloy.

Those surface portions of leads 1c excluding such bump underlayer pattern 1c1 and the surfaces of adhesive 1b are coated with the solder resist 1d. The solder resist 1d is about 20 μm in thickness, by way of example. In the first illustrative embodiment the coat layer of lead 1c is made of the solder resist 1d thereby enabling miniaturization of the diameter of a connection hole for exposure of the bump underlayer pattern 1c1.

On the other hand, the semiconductor chip 2 consists of a small piece of silicon (Si) single-crystal of rectangular planar shape for example, which has its principal surface on which predesigned semiconductor integrated circuitry is formed. In the first embodiment the semiconductor chip 2 is less in

thickness than the tape base 1a of tape carrier 1: The chip thickness is approximately 50 μm for example. This thickness value of the semiconductor chip 2 has been established by applying polishing processes such as for example spin-etching techniques after having abraded the bottom surface of a semiconductor wafer. This makes it possible for the semiconductor chip 2 to become thinner down at 20 to 30 μm as an example. In addition, it is also possible to smoothen the back surface of the semiconductor chip 2, which in turn enables the semiconductor chip 2 to offer anti-crackable structure with enhanced robustness against bending stresses applied thereto.

In addition, the plural bonding pads 2b stated supra are disposed in a region near the longer sides on the principal surface of the semiconductor chip 2. The bonding pads 2b are the electrodes that are for permitting outward extension of electrodes of the semiconductor integrated circuit discussed above toward the outside of the semiconductor chip 2, which are made for example of aluminum (Al) or Al alloys. Each bonding pad 2b has its upper surface on which a corresponding one of the lead-connecting bump electrodes 2a is formed.

The bump electrodes 2a have been formed by wire

bump methods prior to completion of the spin etching process. More specifically, the bump electrodes 2a may be formed in a way which follows: After having coupled bonding wires to the bonding pads 2b using wire bonding methods, those fine-line portions other than spherical or ball-like portions residing on the bonding wires' contact portions are cut and removed away while allowing the balls to be left on the pads 2b. The bump electrodes 2a are electrically connected to ends of TCP's leads 1c in the way stated previously. Additionally, the height of each bump electrode 2a obtained after inner-lead bonding process is about 21.5 μm as an example.

Incidentally, in the first embodiment, the semiconductor chip 2 is coated with the seal resin 3 both on the principal surface and on the bottom or back surface thereof. And, a layout position of the semiconductor chip 2 in a direction along the thickness of tape base 1a is designed so that a stress neutral plane "A" of the overall TCP is substantially identical to a stress neutral plane of the semiconductor chip 2. In other words the semiconductor chip 2 is placed at a specific location whereat any stress being applied from the TCP is minimal. With such an arrangement, even when external

force is applied resulting in deformation of the TCP as a whole, the stress the semiconductor chip 2 might receive remains small while at the same time enabling suppression of warp of the entire TCP due to bimetal effects, which in turn makes it possible to noticeably reduce risks of chip cracks as well as the rate of occurrence of connection deficiency or failure when on-board mount installation of the semiconductor device.

It is noted that the stress neutral plane *A* is the plane parallel to the principal surface of the semiconductor chip 2, which is a specific plane on which the stress applied to the semiconductor chip 2 becomes neutral in the direction along the thickness of the semiconductor chip 2. In Fig. 1 the stress neutral plane *A* is shown by a line segment, which means that it is the parallel plane to the semiconductor chip 2's principal surface at those locations on such line.

The seal resin 3 for use in sealing the semiconductor chip 2 is made of an epoxy-based resin material for example, which is formed such that its upper and lower surfaces are coincident in level with—i.e. coplanar with—the upper and lower surfaces of the tape carrier 1, respectively. To be more

specific, the thickness D1 of the seal resin 3 is equal to the thickness D2 of the tape carrier 1. Whereby, it becomes possible to let the total thickness of the TCP be the thickness of the tape carrier 1. It is thus possible to obtain a thickness-reduced or "thinner" semiconductor device of TCP structure. Additionally, the seal resin 3 has been fabricated by transfer mold methods or else.

An explanation will next be given of a manufacturing method of the semiconductor device in accordance with the first embodiment with reference to Fig. 4 up to and including Fig. 10 below.

First, as shown in Fig. 4, form a device hole 1a1 at a prespecified part of a belt-like tape base 1a with adhesive 1b applied to its one surface.

Subsequently, adhere Cu, for example, to one surface of the tape base 1a by use of the adhesive 1b bonded to the one surface; thereafter, the Cu thin film is patterned by etching techniques or the like to thereby form a plurality of leads 1c as shown in Fig. 5. In this case a bump underlayer pattern 1c1 is formed at part of the leads 1c while simultaneously forming the Cu thin-film layer 1c3 stated above (see Fig. 2).

Thereafter, as shown in Fig. 6, fabricate on the

tape base 1a's one surface a solder resist 1d thus letting the bump underlayer pattern 1c1 and inner lead 1c be exposed to the atmosphere. Then, use the solder resist 1d as a mask to effectuate Au electroplating with respect to those portions of leads 1c exposed from the solder resist 1d. At this process step, Au plating, for example, is also effected to the surface of bump underlayer pattern 1c1 along with the surface of copper thin-film layer 1c3 (see Fig. 2). Whereby, the tape carrier 1 is manufactured.

Subsequently, after placing the semiconductor chip 2 within the device hole 1a1 of the tape base 1a and then performing position alignment between the semiconductor chip 2's bump electrodes 2a and leads 1c, bond the bump electrodes 2a to the leads 1c by simultaneous or "all-at-once" inner lead bonding methods as shown in Fig. 7.

Thereafter, let the tape carrier 1 mounting thereon the semiconductor chip 2 be received in a molding die 5 as shown in Fig. 8; then, inject a molten seal resin material that has been fed into the runner 5b of molding die 5 into the cavity by way of the sub-runner 5c, the gate 5a and the seal resin injection port 1a2 of the tape base 1a, which cavity is formed by the tape base 1a's device hole 1a1 and

the molding die 5. Additionally, air components or "bubbles" residing inside of the cavity are externally exhausted through an air vent which is provided on the seal resin flowout side in the molding die 5.

During this sealing process, in the first embodiment, provision of the passage port 1a2 for use in injecting seal resin may enable uniform flow of the seal resin 3 onto both the principal surface and the back surface of the semiconductor chip 2, which in turn makes it possible to suppress unwanted creation of voids or the like therein.

Then, take the resultant resin-sealed TCP out of the molding die 5. When this is done, in the first embodiment, the plating-treated copper thin-film layer 1a3 is formed at part of the tape base 1a which faces the subrunner 5c thereby enabling reduction of adhesivity of resin residing within the subrunner at such part, which in turn makes it possible to readily remove away residual resin components in the subrunner which can attach to such part.

In this way the intended TCP is manufactured through sealing of the semiconductor chip 2 by use of the seal resin 3 as shown in Fig. 9. In the first embodiment both of the principal surface and back surface of the semiconductor chip 2 are coated with

the seal resin 3. Note that the heights of the seal resin 3's upper and lower surfaces are identical to those of the upper and lower surfaces of tape carrier 1.

Thereafter, the resultant TCP is subject to aging processes and screening inspection procedures as well as cut-into-pieces processes; then, as shown in Fig. 10, let bump electrodes 4 made for example of a Pb-Sn alloy contact the bump underlayer pattern 1c1 of leads 1c.

According to the first illustrative embodiment obtainable in the way stated above, several technical effects and advantages are achievable which follow.

(1) Letting the seal resin 3 coating both the principal surface and back surface of the semiconductor chip 2 may reduce the stress the semiconductor chip 2 can receive from its principal surface and back surface. Especially, setting the location of the semiconductor chip 2 to ensure that the stress neutral plane A of the TCP as a whole is nearly equal to the semiconductor chip 2's stress neutral plane may enable the semiconductor chip 2 to be disposed at an "ideal" position whereat any stress received from the TCP remains minimal to thereby guarantee that the stress the semiconductor chip 2

might receive is small even upon occurrence of deformation of the TCP as a whole due to application of external force while successfully suppressing warp of the entire TCP due to bimetal effects, thus making it possible to greatly reduce risks of chip cracks as well as the rate of occurrence of connection deficiency or failure when on-board mount installation of the semiconductor device.

(2) Providing the tape base 1a with the passage or port 1a2 for use in injecting seal resin which functions as a gate during resin 3 sealing processes may enable uniform injection of the seal resin onto both the principal surface and the rear surface of the semiconductor chip 2, which in turn makes it possible to suppress unwanted creation of voids and/or traps in such seal resin 3.

(3) Provision of the plated copper thin-film layer 1a3 at specified part of the tape base 1a whereat the seal resin can contact during resin seal processes may reduce the adhesivity between residual resin 3 at such part and the tape carrier 1, which in turn makes it possible to facilitate peeloff removal of residual resin components in the subrunner when separation of the TCP from the subrunner after completion of the resin sealing process from the tape carrier 1.

(4) Effectuation of polishing the back surface of the semiconductor chip 2 by spin-etching techniques or the like makes it possible for the semiconductor chip 2 to become thinner down at 20 to 30 μm for example. In addition, it is also possible to smoothen the back surface of the semiconductor chip 2, which in turn enables semiconductor chip 2 to offer anti-crackable structure with enhanced robustness against any bending stress applied thereto.

(5) By performing machining to let the thickness D1 of the seal resin 3 be equal to the thickness D2 of tape carrier 1, it becomes possible to let the total thickness of the TCP be the thickness of the tape carrier 1. It is thus possible to obtain a thickness-reduced or "thinner" semiconductor device of TCP structure than ever.

A semiconductor device in accordance with another embodiment of the present invention will next be explained with reference to Fig. 11.

The semiconductor device of the second embodiment may be the same in basic structure as the said embodiment. A significant difference is that the inner lead portion of a lead 1c is bent in the direction along its thickness causing the inner lead to contact the bump electrode 2a of the semiconductor

chip 2 while it is offset by about 50 μm along the thickness thereof, which results in a stress neutral plane A1 of the semiconductor chip 2 being slightly deviated from the stress neutral plane A of the entire TCP structure.

Note however that from a viewpoint of retaining reliability, relative deviation between the position of the entire TCP's stress neutral plane A and the semiconductor chip 2's stress neutral plane A1 is designed to fall within an allowable range or tolerance zone of ±60 μm. In the second embodiment such deviation is set at 47.5μm, or more or less.

Occurrence of the deviation between the stress neutral planes A, A1 resulted from bending of lead 1c is due to a difference in thickness among constituent components including but not limited to the tape base 1a, height differences of bump electrodes 2a after completion of inner-lead bonding processes, differences in height setup values of a heater tool for use during bonding, and others. In the second embodiment the total thickness of the tape carrier 1 is approximately 250 μm by way of example; the thickness of the tape base 1a is about 150μm for example; the thickness of the adhesive 1b is about 20 μm for instance; the thickness of lead 1c is about 35

μm for instance; the thickness of solder resist 1d is about 25μm as an example; and, the height of bump electrode 4a after execution of inner-lead bonding is about 20μm for example.

Another difference of the second embodiment over the first embodiment is that Sn-plating, for example, is applied to the end of lead 1c, which end is in turn contacted with its associative bump electrode 2a that is made of Au. Accordingly, the lead 1c and bump electrode 2a are contacted together via Au-Sn eutectic junction.

Incidentally, as an application of the second embodiment, the following is also employable. In cases where the stress neutral plane A1 of the semiconductor chip 2 and the stress neutral plane A of the TCP as a whole are little deviated from each other due to any possible thickness differences among respective constituent parts or components of the TCP, such deviation is corrected by adjustment of the bending amount of the lead 1c.

More specifically, the position of the semiconductor chip 2 in the direction along the thickness of the tape base 1a may be set by changing the lead 1c's bend amount in a way such that the semiconductor chip 2's stress neutral plane A1 becomes

identical to the entire TCP's stress neutral plane A. With such an arrangement, even where the TCP's respective components vary in size or else, it becomes possible to set the semiconductor chip 2 at an optimal location at which the stress being applied to the semiconductor chip 2 becomes minimized, in a way responsive to such component size variations.

A semiconductor device in accordance with another embodiment of the instant invention will be described with reference to Fig. 12.

The semiconductor device of the third embodiment is generally similar in structure to the embodiment discussed above. Some significant differences therefrom are as follows.

A first difference lies in that the lead 1c is bent in the direction along its thickness and is directly contacted with its associated bonding pad. The lead 1c has its end surface which has been subject to Au electroplating treatment for example and is coupled by single-point ultrasonic thermo-compression bonding methods to its associated bonding pad made of for example aluminum (Al) or the like.

A second difference is that the other end of lead 1c is designed to extend from the outer periphery of the tape base 1a to have a projected portion of "gull-

wing" shape. In this case, unlike said first embodiment using the external terminal as the bump electrode, it becomes possible to lower the resultant parts mount/assembly height.

A semiconductor device in accordance with another embodiment of this invention will be explained with reference to Fig. 13.

The fourth embodiment is an example adaptable for use in case where liquid resin is dropped down and then subject to thermal hardening to thereby form seal resin 3 as shown in Fig. 13, i.e. what is called the potting seal method.

The seal resin 3 used in this case also is arranged to coat both of the principal surface and back surface of the semiconductor chip 2 for letting the stress neutral planes A, A1 (see Fig. 11) be identical to each other as discussed previously. This seal resin 3 has its thickness which is as large as the thickness D2 of the tape carrier 1 on the side of outer periphery (thickness D1a) of the semiconductor chip 2, and which is gradually reduced or "tapered" toward the center of the semiconductor chip 2 (on the thickness D1b side).

In the fourth embodiment, in addition to the advantages obtained from the first embodiment stated

above, there is obtainable an advantage that the intended resin sealing is achievable without having to use molding dies, which may in turn make it possible to readily seal the semiconductor chip 2 when compared to the cases of said first to third embodiments.

A semiconductor device in accordance with another embodiment of the invention will be explained with reference to Figs. 14-21.

A structure of the semiconductor device of the fifth embodiment will first be set forth in conjunction with Figs. 14 and 15. Note that Fig. 14 is a sectional view taken along line XIV-XIV of Fig. 15. Also note that in Fig. 15 a solder resist and sealing resin are not depicted for purposes of convenience in illustration only.

In the fifth embodiment a plurality of TCPs each similar in structure to the TCP that has been explained in the context of said first embodiment are laminated on one another to constitute a multi-layered TCP structure while causing each TCP's same signal and power supply leads 1c to be electrically connected together via connection sections 6 each penetrating a corresponding one of tape bases 1a of respective TCPs, which connection section 6 is in turn connected to a bump electrode 4 on the TCP bottom surface at the

lowermost layer thereby permitting drawout toward the outside of the multilayer TCP.

Adjacent ones of the laminated unitary TCPs are bonded together by adhesive 1e. This adhesive 1e is a member for constituting part of the unitary TCP's tape carrier 1; for example, it is made of a thermally deformable polyimide resin material. Note however that the leads 1c of the lowermost unitary TCP are coated with a solder resist 1d.

The connection section 6 above is structured from a connection hole 6a and a conductor portion 6b embedded within the connection hole 6a. The connection hole 6a is formed at a selected position in the tape carrier 1 which corresponds to a bump underlayer pattern 1c1 of lead 1c.

It is noted that in the connection holes 6a, the connection hole 6a defined at the bump underlayer pattern 1c1 of lead 1c is formed so that the hole diameter of it is smaller by approximately 50μm, for example, than the hole diameter of the connection hole 6a as defined in the tape base 1a. This is in order to facilitate that part of the bump underlayer pattern 1c1 of lead 1c is projected into inside of the connection hole 6a whereby the conductor portion 6b embedded within the connection hole 6a surely comes

into contact with the lead 1c for achievement of stable electrical connection with the lead 1c. The conductor portion 6b is made of a Pb-Sn alloy by way of example.

With such a multilayer TCP structure it is possible to achieve high-density packaging of the semiconductor chips 2. One example is as follows. Assuming that eight TCPs, each 167μm thick, are stacked in case a 64M-bit dynamic random-access memory (DRAM) for example is formed on one semiconductor chip 2, it becomes possible to obtain a multilayer TCP having in total a storage capacity of 64 megabytes (MB) with the resulting total thickness measuring about 1.3 mm.

Next, a manufacturing method of the semiconductor device in accordance with the fifth embodiment will be explained in conjunction with Figs. 16-21.

First, as shown in Fig. 16, form by mechanical die-punching techniques a device hole 1a1 and connection holes 6a at selected portions of a tape base 1a with adhesive 1b bonded to its one surface.

Subsequently, bond a Cu thin-film for example to one surface of the tape base 1a by using the adhesive 1b attached thereto; thereafter, pattern the Cu thin film by etching methods or the like to thereby form a

plurality of leads 1c while defining in the bump underlayer pattern 1c1 connection holes 6a which are less in diameter than the connection holes 6a at the tape base 1a portions as shown in Fig. 17.

Thereafter, as shown in Fig. 18, provide adhesive 1e made of for example thermally deformable polyimide resin on the side of the copper thin film; then, remove part of such adhesive 1e so that the bump underlayer pattern 1c1 portion of lead 1c and a projected inner lead portion 1c are exposed.

Next, use the adhesive 1e as a mask to apply Au electroplating, for example, to those portions of leads 1c exposed from the adhesive 1e. The tape carrier 1 is thus manufactured.

Subsequently, place a semiconductor chip 2 within the device hole 1a1 of the tape base 1a. Then, perform position alignment between the semiconductor chip 2's bump electrodes 2a and leads 1c. Thereafter, contact the bump electrodes 2a with leads 1c by all-at-once inner-lead bonding techniques as shown in Fig. 19.

Thereafter, place the tape carrier 1 mounting thereon the semiconductor chip 2 within a molding die 5 as shown in Fig. 8; then, inject a molten seal resin material, which has been fed to inside of a runner 5b

of the molding die 5, into a cavity as formed of the tape base 1a's device hole 1a1 and the molding die 5 through a subrunner 5c and a gate 5a as well as a seal resin injection port 1a2 of the tape base 1a. Note that residual air in the cavity is externally exhausted through an air vent which is provided on the seal resin flowout side in the molding die 5. In this case, in the fifth embodiment also, provision of the seal resin injection port 1a2 enables uniform flow of the seal resin onto both the principal surface and the back surface of the semiconductor chip 2, which in turn makes it possible to suppress unwanted creation of voids or else therein.

Then, take the resin-sealed TCP out of the molding die 5. When this is done, in the fifth embodiment also, the plating-applied copper thin-film layer 1a3 is formed at part of the tape base 1a that faces the subrunner 5c thus enabling reduction of adhesivity between resin residing within the subrunner 5c and the tape carrier 1, which in turn makes it possible to readily remove away residual resin components in the subrunner 5c which can attach to such part.

In this way the intended unitary TCP is manufactured through sealing of the semiconductor chip

2 by the seal resin 3 as shown in Fig. 20. In the fifth embodiment also, both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3. Note that the seal resin 3's upper and lower surfaces are identical in height to the upper and lower surfaces of the tape carrier 1, respectively.

Subsequently, the resultant unitary TCP is subject to aging processes and screening inspection procedures as well as cut-into-pieces processes; then, in the fifth embodiment, laminate as shown in Fig. 21 a plurality of such unitary TCPs each of which has been manufactured in the way stated supra while letting respective connection holes 6a be identical in position to one another. Note that the unitary TCP's bottom surface at the lowermost layer is formed with a solder resist 1d rather than the adhesive 1e, which resist is formed in the state that the bump underlayer pattern 1c1 is exposed.

Thereafter, use the adhesive 1e sandwiched between adjacent ones of the unitary TCPs to contact the unitary TCPs together by thermo-compression methods thereby forming the intended multilayer TCP. To make long story short, as multiple unitary TCPs are stacked or laminated on one another by use of the

adhesive 1e that is formed during fabrication of a unitary TCP, it becomes possible to manufacture the multilayer TCP without increasing production process steps required.

Then, fill inside of connection holes 6a of the resultant multilayer TCP with solder paste made of for example Pb-Sn or other similar suitable materials; thereafter, reflow processing is effected thereto thereby forming the conductor portions 6b shown in Fig. 14 within the connection holes 6a. This makes it possible to electrically connect all of the laminated unitary TCPs together at one process step.

Subsequently, let bump electrodes 4 made of Pb-Sn alloy for example contact the bump underlayer pattern 1c1 of leads 1c at the unitary TCP of the lowermost layer of the multilayer TCP, thereby manufacturing the semiconductor device having the multilayer TCP structure of the fifth embodiment.

According to the fifth embodiment obtained in the way stated above, the following technical effects and advantages are achievable in addition to those obtained in said first embodiment.

(1) Constituting the multilayer TCP by lamination of a plurality of thin unitary TCPs makes it possible to greatly improve the packaging density of semiconductor

chips 2 while reducing the total thickness and dimensions of the multilayer TCP.

(2) By bonding together multiple unitary TCPs by using the adhesive 1e that constitutes part of a unitary TCP and is formed during formation of the unitary TCP, it becomes possible to manufacture the multilayer TCP without increasing process steps required.

An explanation will next be given of another embodiment of the invention——a sixth embodiment, which is substantially the same in structure as said fifth embodiment. Significant differences lie in manufacturing methodology of it; hence, the manufacturing method will be explained with reference to Figs. 22-25 below.

First, as shown in Fig. 22, manufacture a unitary TCP in a way similar to that of said first embodiment. This unitary TCP has connection holes 6a as defined to extend through a tape base 1a between its upper and lower surfaces.

Subsequently, as shown in Fig. 23, use print methods to form solder paste 6b1 made for example of Pb-Sn or the like within connection holes 6a of the unitary TCP. After having prepared a predetermined number of similar unitary TCPs, laminate respective

unitary TCPs on one another in the state that their connection holes 6a are aligned in position with one another. And, temporarily secure the laminated unitary TCPs together by utilizing the adhesivity of such solder paste 6b1 within the connection holes 6a of respective unitary TCPs.

Thereafter, apply reflow processing to the resultant multiple unitary TCPs laminated and temporarily fixed together for fusion of the solder paste 6b1 within the connection holes 6a of respective unitary TCPs.

Whereby, conductor portions 6b are formed as shown in Fig. 24 while letting solder paste 6b1 solder paste 6b1 within the connection holes 6a of respective unitary TCPs be integral together, thereby to manufacture a multilayer TCP. As stated above, in the sixth embodiment, it is possible to bond the unitary TCPs together by the conductor portions 6b, rather than by means of adhesive.

Finally, as shown in Fig. 24, let bump electrodes 4 made for example of Pb-Sn or else be in contact with the bump underlayer pattern 1c1 of leads 1c at the unitary TCP of the lowermost layer of the multilayer TCP to thereby manufacture a semiconductor device having the multilayer TCP structure of the sixth

embodiment.

A semiconductor device in accordance with another embodiment of the present invention will be described in conjunction with Figs. 26-30.

First, a structure of the semiconductor device of the seventh embodiment will be explained with reference to Fig. 26. Note that a plan view of the semiconductor device of the seventh embodiment is the same as Fig. 15 which has been used in explanation of said fifth embodiment.

In the seventh embodiment the multilayer TCP's seal resin 3 is not separated in units of individual tape carriers 1, but is designed so that the resin is integrally molded to have a structure for sealing plural semiconductor chips 2 together. In addition, the plating-effected copper thin-film layer 1a3 stated above is formed in a limited region of the lowermost layer's tape base 1a in close proximity to the seal resin injection port 1a2 (the same position as said first and fifth embodiments). The remaining structure is the same as that of said fifth embodiment.

In the semiconductor device of the seventh embodiment above, since no gaps are formed between layers of seal resin 3 each for use in sealing the individual semiconductor chip 2, it becomes possible

to improve the mechanical strength of a multilayer package when compared to said fifth embodiment while increasing the moisture vapor resistivity or humidity durability.

A manufacturing method of the semiconductor device of the seventh embodiment will be explained with reference to Figs. 27-30. Note that the manufacturing steps of tape carriers in the seventh embodiment is the same as those which have been explained using Figs. 16-18 in the context of said fifth embodiment, any duplicative description will be eliminated herein. Also note that Fig. 29 is a sectional view taken along line XXIX-XXIX of Fig. 15.

First, as shown in Fig. 27, place a semiconductor chip 2 within a device hole 1a1 of a tape base 1a; then, after performing positional alignment between bump electrodes 2a of the semiconductor chip 2 and leads 1c, all-at-once inner lead bonding is effected letting the bump electrodes 2a contact the leads 1c.

Subsequently, after lamination of a plurality of tape carriers 1 each mounting thereon its semiconductor chip 2 as shown in Fig. 28, use the adhesive 1e between tape carriers 1 to temporarily secure resultant carriers together by thermo-compression bonding methods.

Here, in the seventh embodiment, seal resin injection ports 1a2 of the laminated tape bases 1a are identical in planar position in a manner such that each port is formed extending in the direction along the thickness of the stacked tape bases 1a. A certain unitary TCP at the lowermost layer of the multilayer structure is formed with a solder resist 1d, rather than the adhesive 1e, while allowing the bump underlayer pattern 1c1 be exposed therefrom.

Thereafter, as shown in Fig. 29, place the stacked tape carriers 1 within a molding die 5. This molding die 5 is of the structure which enables simultaneous sealing of respective semiconductor chips 2 within the tape carriers 1 laminated.

Then, inject a molten seal resin material, which has been supplied to inside of a runner 5b of the molding die 5, into a cavity as formed by the tape base 1a's device hole 1a1 and the molding die 5 by way of a subrunner 5c and a gate 5a plus a seal resin injection port 1a2 of the tape base 1a. Note that the air residing within the cavity is externally exhausted through an air vent which is provided on the seal resin flowout side in the molding die 5.

In this case, in the seventh embodiment, it is possible to allow the molten seal resin as injected

from the gate of the molding die 5 flow uniformly onto the principal surface and the back surface of semiconductor chip 2 through the seal resin injection port 1a2 extending in the direction along the thickness of the tape base 1a. This in turn makes it possible to suppress unwanted creation of voids or else in the seal resin 2 of the multilayer TCP. In other words it is possible to simultaneously seal respective semiconductor chips 2 of the laminated tape carriers 1 while retaining them in the stable state. Additionally, arrows in Fig. 29 designate flow directions of the molten seal resin.

Then, unload from the molding die 5 the resulting TCP after completion of the resin sealing process. When this is done, in the seventh embodiment, the plating-effected copper thin-film layer 1a3 is formed at part of the tape base 1a of the lowermost layer which faces the subrunner 5c thereby enabling reduction of adhesivity of the seal resin 3 at such part, which in turn makes it possible to readily remove away any residual resin components attached to such part.

In this way a multilayer TCP is manufactured by sealing all of the multiple semiconductor chips 2 by the seal resin 3 at a time as shown in Fig. 30. In

the seventh embodiment also, both of the principal surface and back surface of each semiconductor chip 2 are well coated with the seal resin 3. Note that the seal resin 3 is formed so that it is coincident in upper and lower surface levels with the tape carrier 1.

Subsequently, the laminated TCP is subject to aging processes and screening inspection procedures plus cut-into-pieces processes; then, fill the connection holes 6a of such laminated TCP with solder paste made for example of Pb-Sn or other similar suitable materials.

Thereafter, apply reflow processing to the stacked TCP to form in the connection holes 6a the conductor portions 6b which have been indicated in Fig. 26; then, let the bump electrodes 4 made for example of Pb-Sn or the like be contacted with the bump underlayer pattern 1c1 of leads 1c at the tape carrier 1 of the lowermost layer of the multilayer TCP to thereby manufacture a semiconductor device having the multilayer TCP structure of the seventh embodiment.

According to the seventh embodiment above, the following technical effects and advantages are achievable in addition to those obtained in said fifth

embodiment.

(1) Integral molding of the seal resin 3 of the multilayer TCP results in no gaps being formed between layers of seal resin 3 each for use in sealing the individual semiconductor chip 2, it becomes possible to improve the mechanical strength of a multilayer package when compared to said fifth embodiment while at the same time enhancing the humidity durability. Thus, it is possible to improve the reliability of the semiconductor device.

(2) Simultaneous fabrication of the seal resin 3 of the multilayer TCP may enable reduction of the manufacturing process steps in number.

A semiconductor device in accordance with another, eighth embodiment of the present invention will next be explained with reference to Figs. 31-32. Note that Fig. 31 shows a sectional view taken along line XXXI-XXXI of Fig. 32. Note also that in Fig. 32 a solder resist and sealing resin are not depicted for purposes of convenience in illustration only.

The eighth embodiment being explained herein is the one which applies the principles of this invention to a dynamic random access memory (DRAM) by way of example, wherein the semiconductor device is generally similar in structure to said fifth embodiment stated

supra.

In Fig. 32 the reference characters "Vcc," "Vss," "I/O," "RAS," "CAS," "WE," "OE," and "Address" are used to designate some major signals and power supply potentials which are allocated to respective leads 1c: "Vcc" designates a high-potential power supply voltage; "Vss" denotes a low-potential power supply voltage; "I/O" indicates an input/output signal; "RAS" shows a row address strobe signal; "CAS" is a column address strobe signal; "WE," a write enable signal; "OE," output enable signal; "Address," an address signal.

Incidentally, in the eighth embodiment shown herein, four CAS bonding pads 2b1 are substantially centrally disposed on a semiconductor chip 2, which pads function as chip select terminals. These CAS bonding pads 2b1 are electrically connected by in-chip leads on the semiconductor chip 2.

And, certain one of such four CAS bonding pads 2b1 has a bump electrode 2a provided thereon, through which bump the pad is electrically connected to its associated lead 1c. In other words the bonding pad 2b1 for chip select is provided with the bump electrode 2a for electrical connection with the lead 1c.

The remaining CAS bonding pads 2b1, however, have no such bump electrodes corresponding to the one 2a, none of these pads are electrically coupled to leads 1c. In other words, in the eighth embodiment, connection path or route is modifiable by specifying whether the bump electrode 2a is provided on a bonding pad 2b. With such an arrangement, the use of a single type of tape carrier 1 may flexibly accommodate any desirable lead pattern modifications occurring in cases of employing multilayer TCP structures without having to newly prepare a separate "special purpose" tape carrier 1 which meets a design change on a case-by-case basis. This makes it possible to avoid the need for redoing of design and manufacture plus inspection of a tape carrier 1 whenever the connection route is altered, which may in turn drastically reduce the time as taken for manufacture of products while reducing production costs.

In addition, although in the above example the connection route is rendered modifiable depending on presence or absence of the bump electrode 2a, the present invention should not be limited to this arrangement only. For example, in case the distal end of Au-plated lead 1c is connected to its associated bonding pad 2b in the absence of a bump electrode 2a

laid therebetween as has been explained in the context of said third embodiment, bonding is eliminated with respect to a specific bonding pad 2b that is free from chip select events when letting the lead 1c be contacted with the bonding pad 2b using single-point bonding methods. In short the connection route may be changed by single-point bonding operations.

In this way, according to the eighth embodiment, the following advantage is achievable in addition to those obtained by said fifth embodiment.

(1) By modifying the connection route by specifying whether the bump electrode 2a is provided on a bonding pad 2b, the use of a single type of tape carrier 1 may flexibly accommodate any desirable lead pattern modifications occurring in the case of employing multilayer TCP structures without having to newly prepare a separate tape carrier 1 which meets a specific design change on a case-by-case basis. This makes it possible to reduce the time required to manufacture products while reducing costs.

A semiconductor device in accordance with another, ninth embodiment of the present invention will next be explained with reference to Fig. 33.

In the ninth embodiment the leads 1c are designed to extend from lateral surfaces of a tape carrier 1 at

each of those layers constituting a multilayer TCP to have the so-called "gull-wing" shape for electrical connection with lands 7a on a printed circuit board 7 used.

A semiconductor device in accordance with another, tenth embodiment of the invention will next be explained with reference to Fig. 34.

In the tenth embodiment the leads 1c are designed to extend from lateral surfaces of a tape carrier 1 at the lowermost layer of those layers constituting a multilayer TCP to have the gullwing-like shape for electrical connection with lands 7a on a printed circuit board 7 used.

A semiconductor device in accordance with another, eleventh embodiment of this invention will next be explained with reference to Fig. 35.

In the eleventh embodiment a conductive pin 6c that is inserted into a connection hole 6a as formed in each tape carrier 1 of a multilayer TCP is rigidly secured by a conductor portion 6b filled within the connection hole 6c to thereby form a connection section 6.

This conductive pin 6c electrically connects between those leads 1c of the same electrical function of a tape carrier 1 of each layer while at the same

time having its one end that extends from the lower surface to form an external terminal. Summarizedly, permitting insertion of the projected portion of this conductive pin 6c into a connection hole of a mount board such as a printed circuit board may result in the multilayer TCP being mounted on the board while letting semiconductor chips 2 within the multilayer TCP be electrically connected to leads of the mount board.

In this way, in the eleventh embodiment, the following advantages are attainable in addition to those obtained by said fifth embodiment.

(1) Letting external terminals be conductive pins 6c may reduce costs of products when compared to the case where such external terminals are constituted from bump electrodes or gullwing-shaped leads.

(2) Inserting strength-enhanced conductive pins 6c into connection holes 6c of the multilayer TCP makes it possible to improve the strength of the multilayer TCP as a whole.

A semiconductor device in accordance with another, twelfth embodiment of the present invention will next be explained with reference to Figs. 36-39.

In the twelfth embodiment, as shown in Fig. 36, leads 1c are formed so that these are projected from

lateral surfaces of tape carriers 1 at respective layers constituting a multilayer TCP and are bent downwardly in Fig. 36, corresponding ones of which are then "bundled" together at their distal ends in a stacked fashion on lands 7a of a mount board, typically a printed circuit board.

The stack-bundled leads 1c exhibit spring-like deformability to relatively easily increase the mechanical strength of the structure of such leads 1c at low costs while simultaneously enabling absorption of stress occurring due to differences in thermal expansion between the multilayer TCP and the mount substrate 7. It is thus possible to increase the reliability of the semiconductor device after on-board installation.

A manufacturing method of the semiconductor device of the twelfth embodiment will be next described with reference to Figs. 37-39.

First, as shown in Fig. 37, laminate and bond together a plurality of unitary TCPs in a way similar to that in said fifth embodiment to thereby fabricate a multilayer TCP. At this stage of fabrication procedures, the leads 1c are extended straightly from lateral surfaces of respective tape carriers 1.

Subsequently, press from the upward direction

against the leads 1c extending straightly from side surfaces of respective tape carriers 1 of the multilayer TCP to machine all of the plural leads 1c at a time into the state in which corresponding ones of such leads 1c's distal ends overlap one another as shown in Fig. 38.

Thereafter, cut away the ends of leads 1c as bent through the machining process thus letting the stacked ends of leads 1c be aligned in position so that the semiconductor device of the twelfth embodiment is manufactured.

According to the twelfth embodiment obtained in the way stated above, the following advantages may be achieved in addition to those derived from said fifth embodiment.

(1) It becomes possible to relatively readily improve the mechanical strength of the lead structure at low costs.

(2) Effecting machining with the outer lead portions of leads 1c resiliently bent makes it possible to well compensate for or "absorb" any possible thermal expansion differences between the multilayer TCP and the mount substrate 7 such as a printed circuit board.

A semiconductor device in accordance with another, thirteenth embodiment of the invention will

next be explained with reference to Figs. 40 and 41. Note that Fig. 41 is a sectional view taken along line XXXXI-XXXXI of Fig. 40, which shows a sectional view of a semiconductor chip and a machining metal mold tool at a resin sealing process step.

In the thirteenth embodiment, as shown in Fig. 40 and Fig. 41, an air exhaust port 1a4 is formed on a tape base 1a at a location on a shorter side of a device hole 1a1 which is the opposite side of the seal resin injection port 1a2 discussed above, the air exhaust port 1a4 extending from the device hole 1a1 in a direction toward a short outer side of the tape base 1a. This air exhaust port 1a4 is formed to resemble the letter "T" in its planar shape, for example.

This air exhaust port 1a4 is an opening for use in coupling between the air vent of the molding die 5 and the cavity, which opening is provided for flowing extra molten resin thereinto thereby forcing air components residing within the cavity to escape to outside of the cavity. In other words the air exhaust port 1a4 offers functionality as part of the air vent during resin sealing processes. Additionally, it will be permissible that the resin contains therein air within the air exhaust port 1a4.

It is thus possible to suppress residence of air

holes or "bubbles" within the seal resin 3 for use in coating both the principal surface and back surface of semiconductor chip 2, which in turn enables significant reduction of unwanted creation of voids and/or traps in the seal resin 3.

It is noted that arrow in Fig. 41 designates the flow direction of the seal resin 3. Also note that in case the tape base 1a is used to constitute the multilayer TCP as has been explained with regard to said fifth embodiment and the like, more than one connection hole may be defined at a selected location corresponding to the lead 1c's bump underlayer pattern 1c1.

According to the thirteenth embodiment obtained in the way stated above, the following advantage is achievable in addition to those obtained by said first and fifth embodiments.

(1) Providing at the opposite shorter side of the device hole 1a1 on the tape base 1a the air exhaust port 1a4 extending from the device hole 1a1 toward the short outer periphery of the tape base 1a and functioning as part of the air vent makes it possible to greatly suppress residence of air holes or "bubbles" within the seal resin 3 for use in coating both the principal surface and back surface of the

semiconductor chip 2, which may in turn enable significant reduction of unwanted creation of voids and/or traps in the seal resin 3. This in turn makes it possible to further increase the reliability of the semiconductor device.

So far, the present invention made by the inventors named in the subject application for patent has been described in detail based on some specific preferred embodiments thereof, it will be understood by those skilled in the art that the invention should not be limited to said first to thirteenth embodiments only, and may be modifiable and alterable in a variety of possible forms without departing from the spirit and scope of the invention.

For example, although in said fifth embodiment or else the solder paste is filled into connection holes for connecting between the unitary TCPs of the multilayer TCP, the invention should not be limited only to this arrangement and may alternatively be modified so that conductive resin paste, for example, is filled in place thereof. If this is the case, after fulfillment of such conductive resin paste inside of connection holes, thermal hardening treatment is done forming a thermally hardened paste material within connection holes to thereby achieve

the intended electrical interconnection between respective unitary TCPs.

Still alternatively, conductor portions within such connection holes may be formed by electroplating techniques. In this case formation of the conductor portions may be made easier because of the fact that traditionally employed plating processing is used to form such conductor portions in the connection holes.

INDUSTRIAL APPLICABILITY

As has been described above, the semiconductor device incorporating the principles of the invention is adaptable for use as a semiconductor device built in electronic equipment including but not limited to computers, portable radiotelephone handsets, or video cameras or else and also in integrated circuit (IC) cards as well as memory cards.

What is claimed is:

1. A semiconductor device including a semiconductor chip disposed in a device hole provided in a tape carrier with one end of a lead on said tape carrier being electrically connected to an external terminal of said semiconductor chip, characterized in that said semiconductor chip is less in thickness than said tape carrier, and that said semiconductor chip is sealed by a seal resin material letting a principal surface and a back surface of said semiconductor chip be coated therewith.

2. The semiconductor device as recited in claim 1, characterized in that said semiconductor chip is disposed on a stress neutral plane extending parallel to the principal surface of said semiconductor chip at a position along a thickness of said tape carrier.

3. The semiconductor device as recited in claim 1, characterized in that said lead is bent in its thickness direction to be electrically connected to said external terminal.

4. The semiconductor device as recited in claim 1, characterized in that said seal resin material has its upper and lower surfaces substantially identical in level to upper and lower surfaces of said tape carrier.

5. The semiconductor device as recited in claim 1, characterized in that a passage for use in seal resin injection is formed at part of said tape carrier thereby causing said device hole to be coupled to a gate of a metal mold structure used during formation of said seal resin.

6. The semiconductor device as recited in claim 5, characterized in that said tape carrier has an air exhaust port as formed letting the device hole of said tape carrier be coupled to an air vent of the metal mold structure for use during formation of said seal resin.

7. The semiconductor device as recited in claim 5, characterized in that an electroplated metal layer is formed at part of a surface of said tape carrier in close proximity to said passage for seal resin injection, the part being brought into contact with seal resin during formation of said seal resin.

8. The semiconductor device as recited in claim 1, characterized in that said tape carrier has an air exhaust port as formed letting the device hole of said tape carrier be coupled to an air vent of a metal mold structure for use during formation of said seal resin.

9. The semiconductor device as recited in claim 1, characterized in that a bump electrode is provided

at a remaining end of said lead for being electrically connected to a lead of a mount board for mounting thereon the semiconductor device.

10. The semiconductor device as recited in claim 1, characterized in that said lead has its other end extending from an outer periphery of said tape carrier to thereby form an outer lead section as electrically connected to more than one lead of a mount board for use in mounting thereon the semiconductor device.

11. The semiconductor device as recited in claim 1, characterized in that said semiconductor chip has its back surface polished by a spin etching technique.

12. The semiconductor device as recited in claim 1, characterized in that said tape carrier is less than or equal to 300 micrometers (μm) in thickness whereas said semiconductor chip is 150 μm or less in thickness with a relative deviation amount between a stress neutral plane of said semiconductor chip and a stress neutral plane of the whole of said semiconductor device falling within a range of $\pm 60 \mu$m.

13. The semiconductor device as recited in claim 1, characterized in that a gold bump electrode is provided at an external terminal of said semiconductor chip, said gold bump electrode being coupled to one end of said lead.

14. The semiconductor device as recited in claim 1, characterized in that electroplating is applied to one end of said lead causing the lead end to be directly coupled to an external terminal of said semiconductor chip.

15. A semiconductor device characterized by having a multilayer package structure including a plurality of laminated tape carriers with a semiconductor chip less in thickness than each said tape carrier being disposed in a device hole of each said tape carrier, wherein one end of a lead provided to each of said plurality of laminated tape carriers is electrically connected to an external terminal of the semiconductor chip in the device hole of each said tape carrier, wherein each said semiconductor chip is coated with seal resin on both of a principal surface and a back surface thereof, and wherein each of said tape carriers laminated has a common signal transmission lead and a power supply lead each being electrically connected to corresponding ones of other carriers to be externally drawn out as a connection terminal being electrically connected to a lead of a mount board.

16. The semiconductor device as recited in claim 15, characterized in that said multilayer package

structure comprises a plurality of unitary packages laminated on one another, and that each said unitary package includes a tape carrier having a device hole with a semiconductor chip disposed therein and sealed by seal resin while letting one end of said lead be electrically connected to an external terminal of said semiconductor chip.

17. The semiconductor device as recited in claim 15, characterized in that said multilayer package structure is configured letting respective ones of said semiconductor chips are sealed by same seal resin as machined simultaneously.

18. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while burying a conductive material within the connection hole letting a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to corresponding ones of remaining carriers, respectively.

19. The semiconductor device as recited in claim 18, characterized in that a bump electrode is provided as said connection terminal at one end of the conductive material buried in said connection hole.

20. The semiconductor device as recited in claim 18, characterized in that part of said lead is projected into said connection hole.

21. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while applying electroplating to inside of the connection hole thus letting each of a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to corresponding ones of remaining carriers.

22. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while inserting a conductive pin into the connection hole thus letting each of a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to corresponding ones of remaining carriers with one end of said conductive pin being extended from a mount surface of said multilayer package as said connection terminal.

23. The semiconductor device as recited in claim

15, characterized by letting a remaining end of a lead of each of said plurality of tape carriers laminated on one another extend from an outer periphery of each said tape carrier to provide a projected lead portion being bent for lamination with others to thereby permit electrical connection between a common signal line of each of said plurality of tape carriers laminated and corresponding ones of other tape carriers and also between a power supply line of each said tape carrier and corresponding ones of other carriers.

24. The semiconductor device as recited in claim 15, characterized by preventing the bump electrode from contact with a certain external terminal of said semiconductor chip to permit modification of a connection route between said semiconductor chip and lead.

25. A method for manufacturing a semiconductor device including a semiconductor chip disposed in a device hole provided in a tape carrier with one end of a lead of said tape carrier being electrically connected to an external terminal of said semiconductor chip, said method characterized by comprising the steps of:

(a) preparing a tape carrier of a specified

thickness with leads disposed around said device hole;

(b) preparing a semiconductor chip less in thickness than said tape carrier chip and having more than one external terminal;

(c) disposing said semiconductor chip thinner than said tape carrier within the device hole of said tape carrier and then electrically connecting the external terminal of said semiconductor chip to one end of said lead; and

(d) effecting sealing by seal resin thereby letting said semiconductor chip be coated therewith on both a principal surface and a back surface thereof.

26. The semiconductor device manufacturing method as recited in claim 25, characterized in that said step of effecting sealing includes injecting said seal resin into the device hole from a gate of a metal mold through a seal resin injection passage as formed on said tape carrier.

27. The semiconductor device manufacturing method as recited in claim 25, characterized by comprising the steps of:

(a) forming a connection hole in said tape carrier causing part of said lead to be exposed from an inner wall surface; and

(b) laminating a plurality of unitary packages

each formed at said sealing step on one another with a formation position of said connection hole kept identical thereby forming a multilayer package.

28. A method for manufacturing a semiconductor device as recited in claim 27, characterized by comprising the steps of:

(a) burying prior to lamination of said plurality of unitary packages a conductive paste within a connection hole of each tape carrier; and

(b) After formation of the multilayer package by lamination of the unitary packages each with said conductive paste buried therein, applying thermal processing to said multilayer package for permitting fusion of the conductive paste within the connection hole being defined in each said tape carrier to provide integration.

29. The semiconductor device manufacturing method as recited in claim 27, characterized by comprising the steps of:

(a) laminating by adhesive said unitary packages on one another to form a multilayer package;

(b) burying a conductive paste within a connection hole as defined in each tape carrier of said multilayer package; and

(c) applying thermal processing to said

multilayer package.

30. The semiconductor device manufacturing method as recited in claim 25, characterized in that external terminals of said semiconductor chip are contacted with leads by a single-point bonding technique while preventing a certain external terminal of said external terminals from contact with a specified lead.

31. A method of manufacturing a semiconductor device characterized by comprising the steps of:

(a) preparing a tape carrier of a specified thickness with leads disposed around said device hole;

(b) preparing a semiconductor chip less in thickness than said tape carrier chip and having more than one external terminal;

(c) disposing said semiconductor chip thinner than said tape carrier within the device hole of said tape carrier and then electrically connecting the external terminal of said semiconductor chip to one end of said lead; and

(d) after lamination of a plurality of tape carriers each with said external terminal electrically connected to the lead, sealing respective semiconductor chips disposed within device holes of respective tape carriers using seal resin at a time.

32. The semiconductor device manufacturing method as recited in claim 31, characterized in that at said sealing step said seal resin is injected into each device hole from a gate of a metal mold by way of a seal resin injection passage as formed at part of each said tape carrier.

ABSTRACT OF THE DISCLOSURE

A semiconductor chip 2 is disposed within a device hole as formed in a tape base material 1a of a tape carrier 1, which chip is less in thickness than the tape base material 1a, while sealing by a seal resin 3 to permit both the principal surface and back surface of such semiconductor chip 2 to be coated therewith. And, let the position of the semiconductor chip 2 in a direction along the thickness of the tape base 1a be identical to a stress neutral plane of the TCP as a whole.

FIG. 1

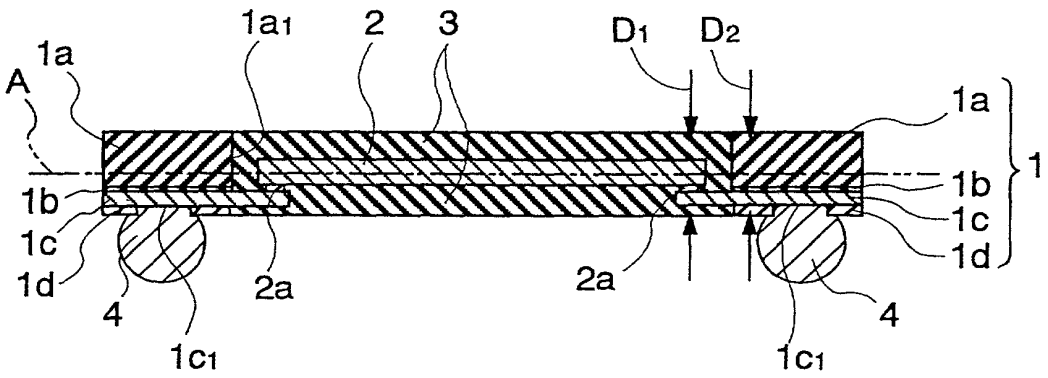
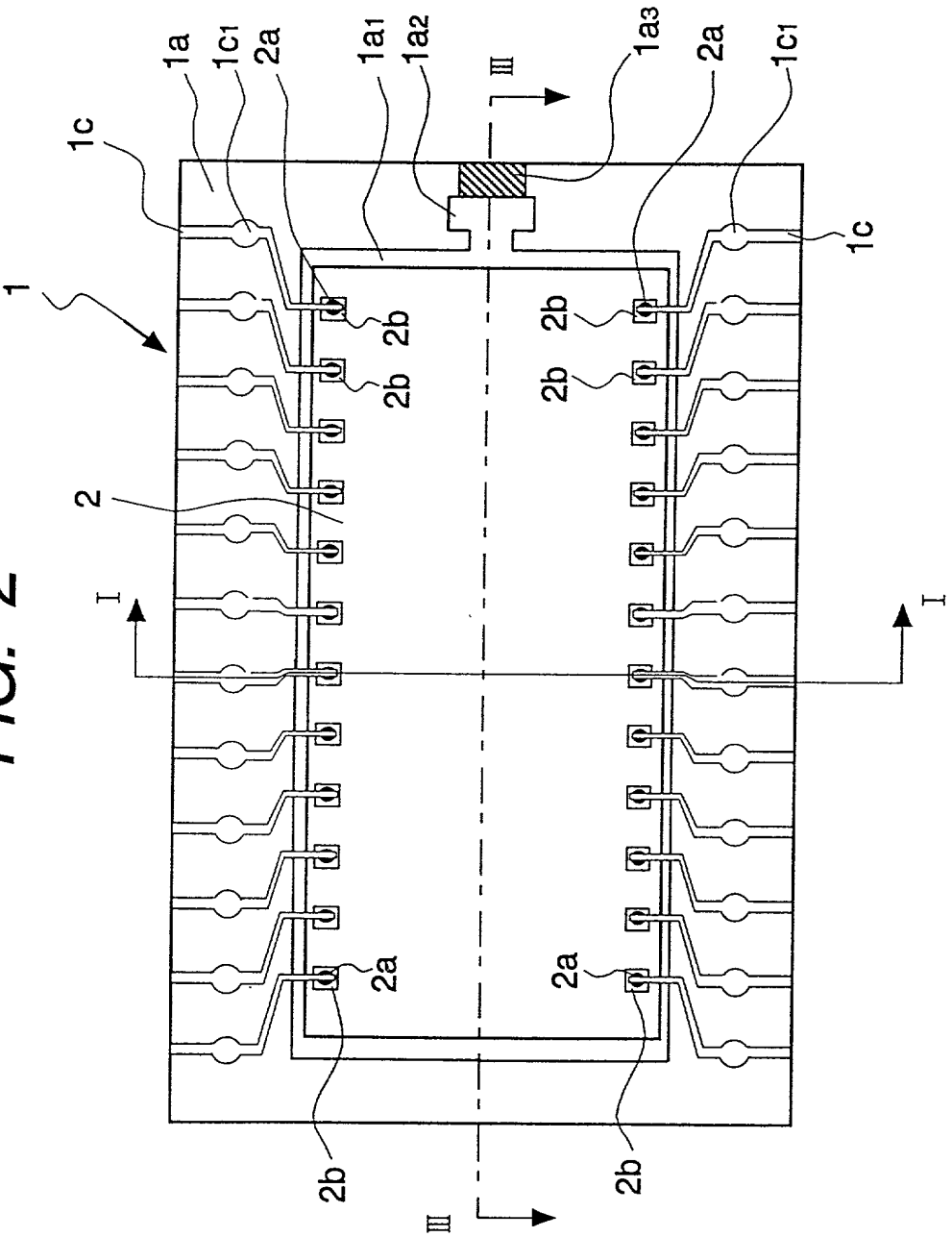


FIG. 2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1a
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2a
1a1
1a2
III
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2a
1c1
1c
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I
I
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2a
2b
2b
III

FIG. 3

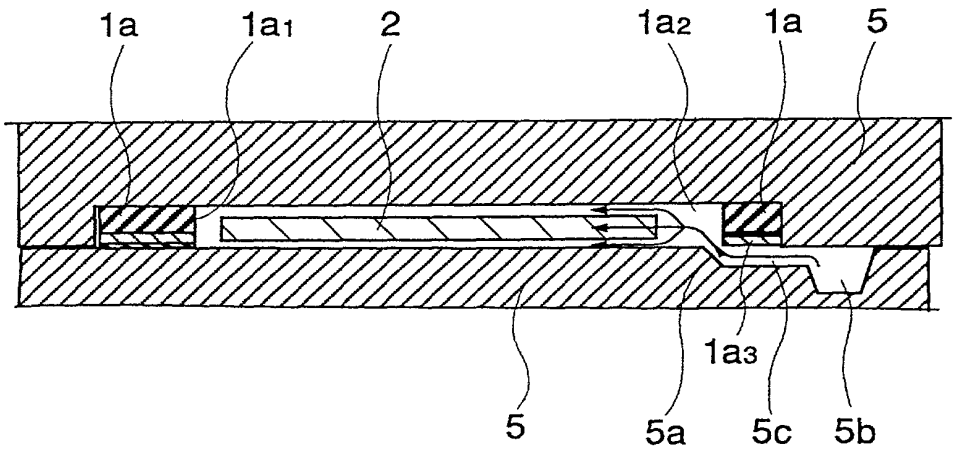


FIG. 4

FIG. 5

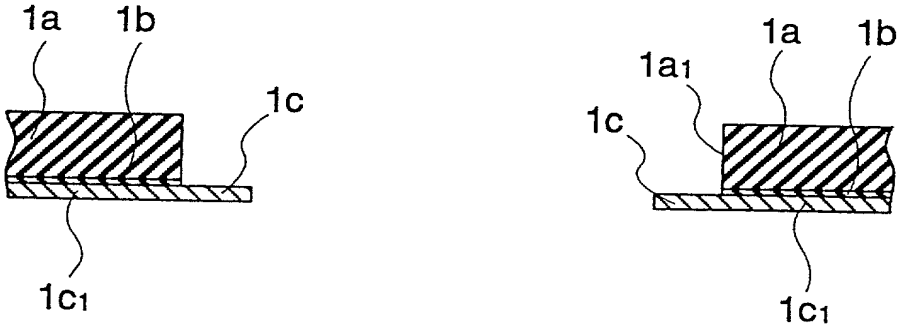
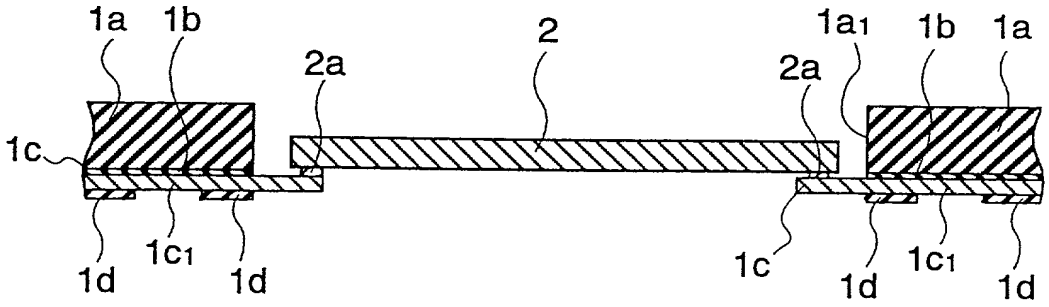


FIG. 6


1a
1b
1c
1d
1c1
1d
1
1a1
1b
1a
1c
1d
1c1
1d

FIG. 7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1b
2a
2
1c
1d
1c1
1d
1a1
1b
1a
2a
1c
1d
1c1
1d

FIG. 8

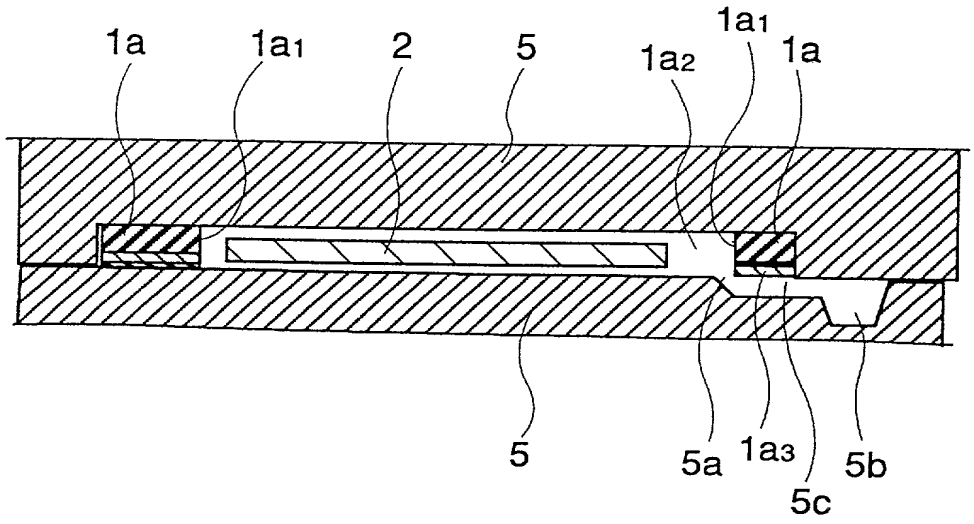
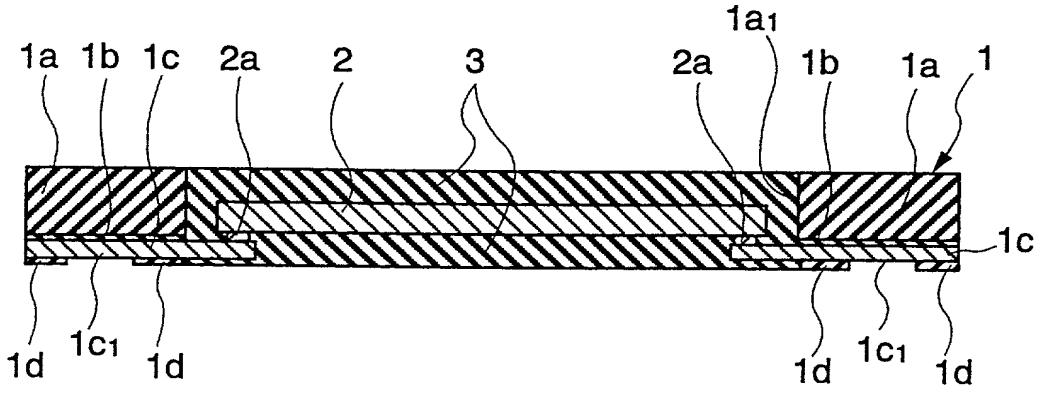


FIG. 9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1b
1c
2a
2
3
2a
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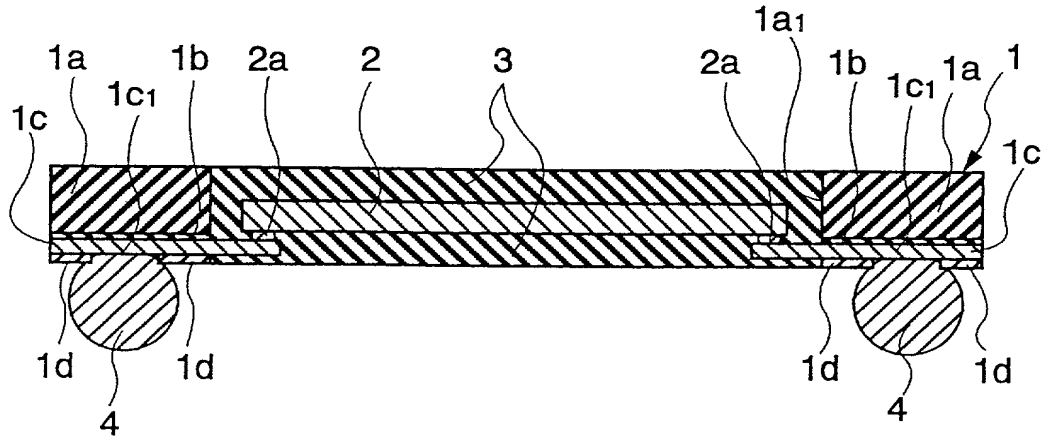
1b
1a
1
1c
1d
1c1
1d
1d
1c1
1d

FIG. 10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2a
2
3
2a
1a1
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1
1c
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1c
1d
1d
4
1d
1d
4

FIG. 11

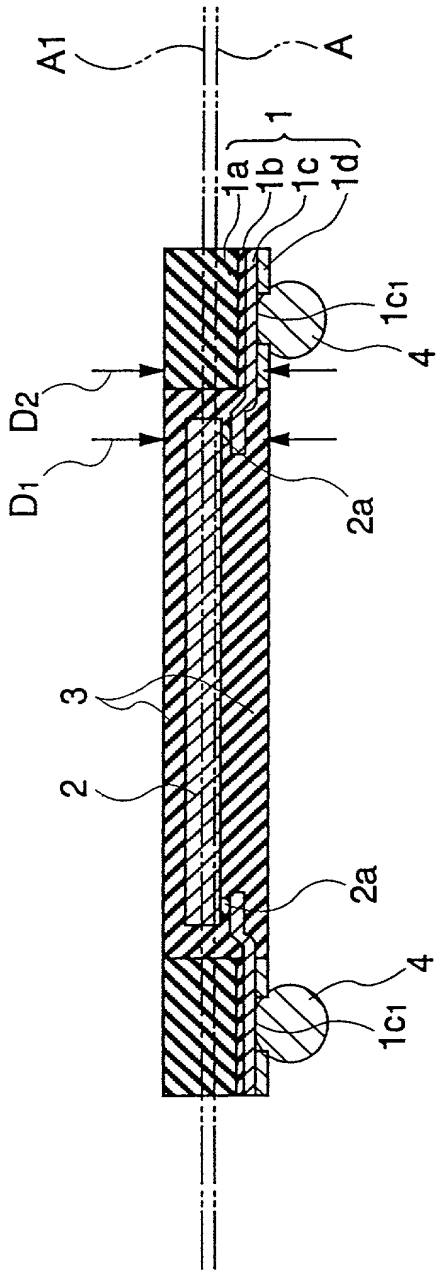


FIG. 12

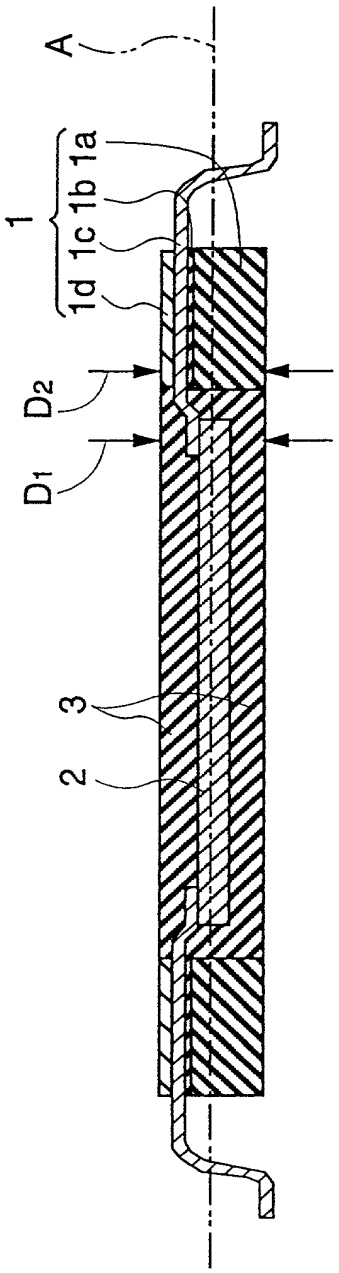


FIG. 13

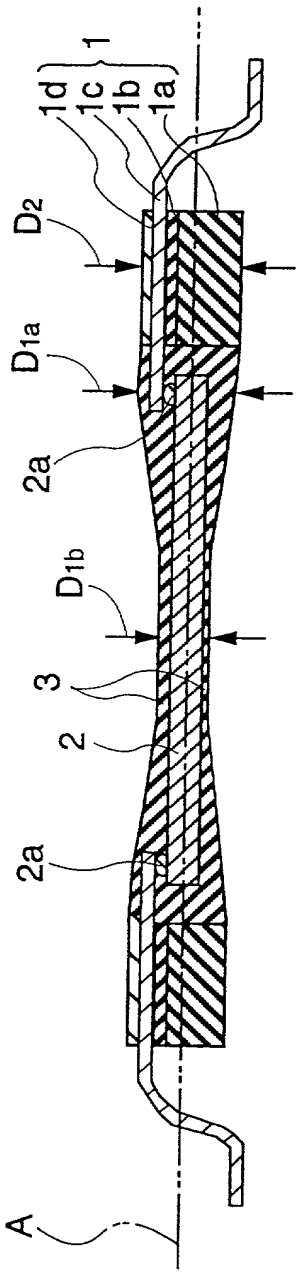


FIG. 14

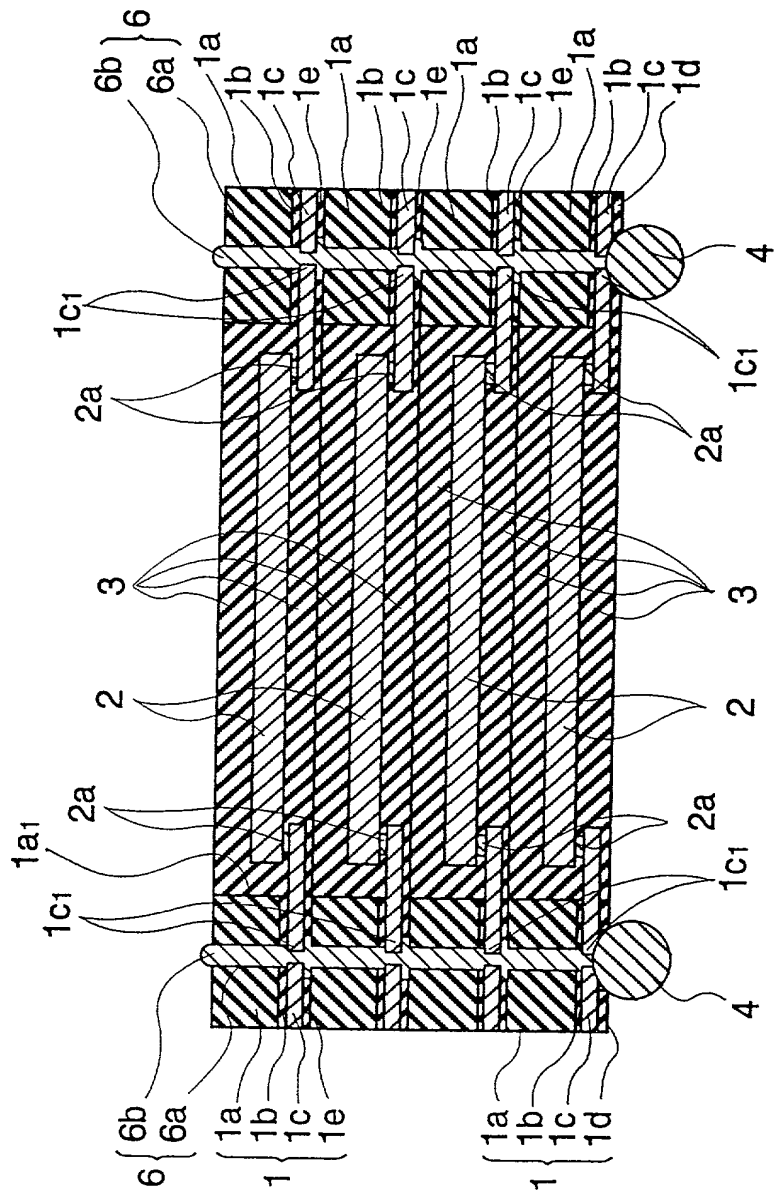
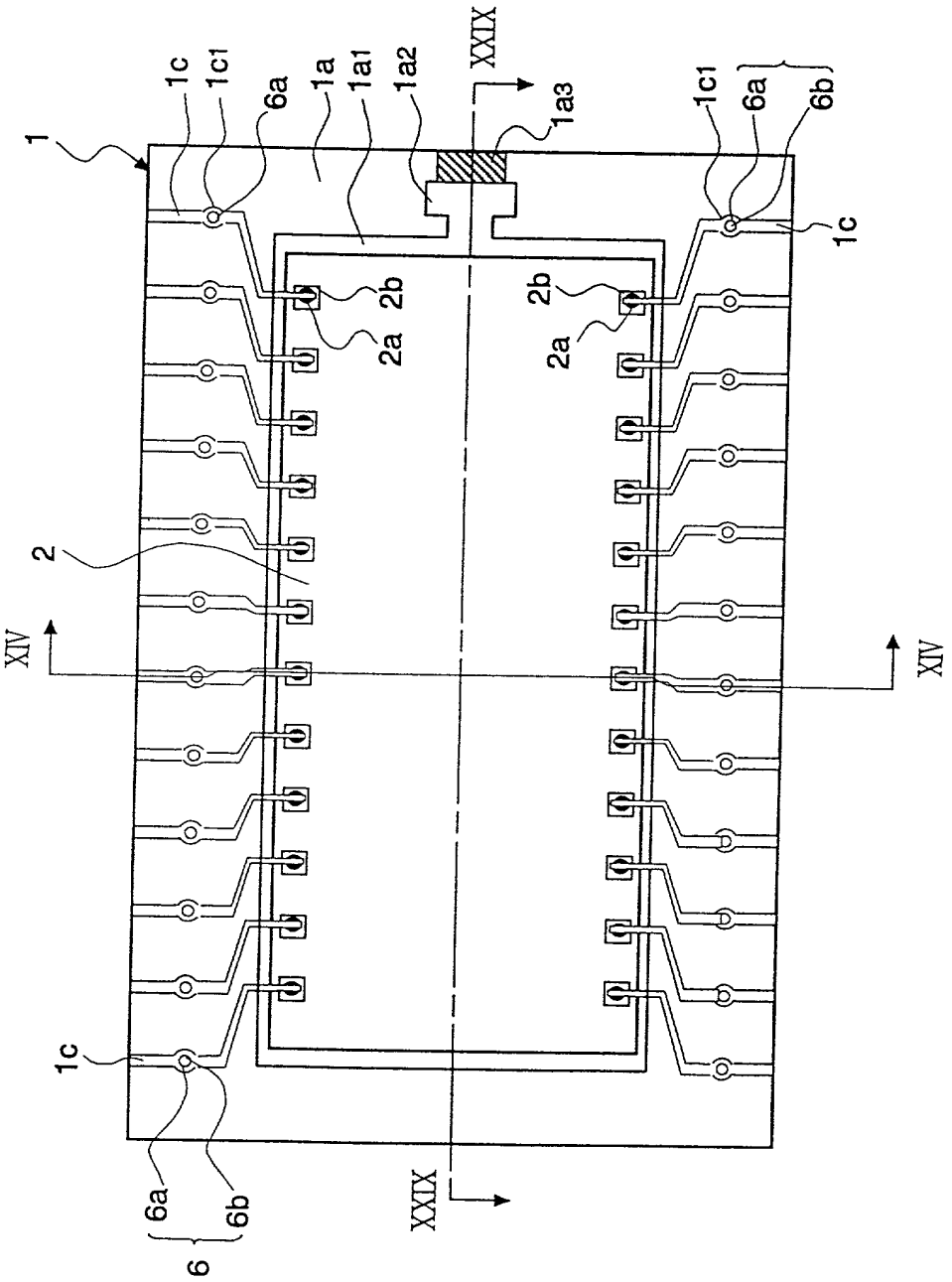


FIG. 15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1c
1c1
6a
1a
1a1
1a2
XXIX
1a3
1c1
6a
6b
1c
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2a
2b
2a
2
XIV
XIV
1c
6a
6b
6
XXIX

FIG. 16

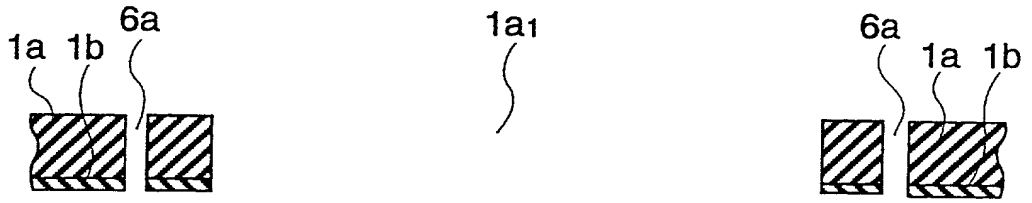


FIG. 17

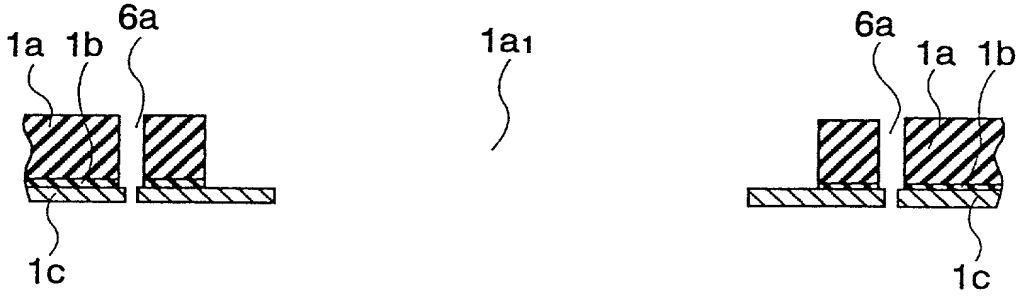
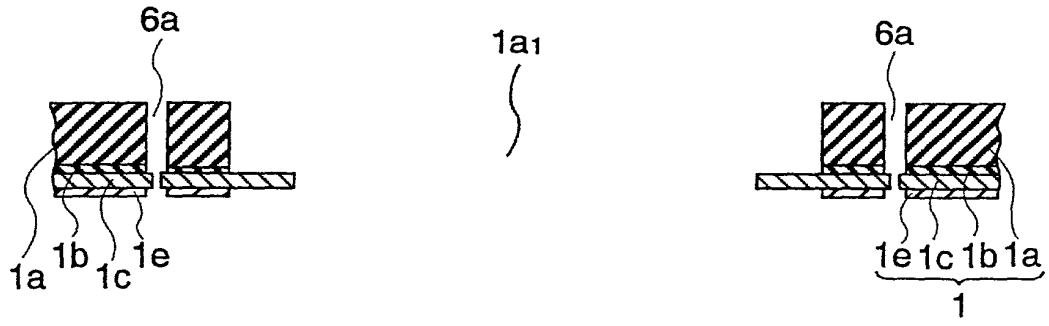


FIG. 18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1a1
6a
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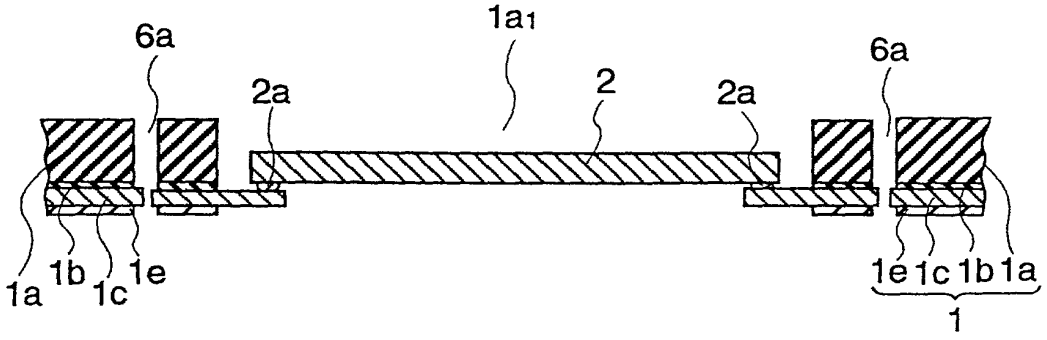
1b
1c
1e
1e
1c
1b
1a
1

FIG. 19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2a
6a
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1c
1e
1e
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1b
1a
1

FIG. 20

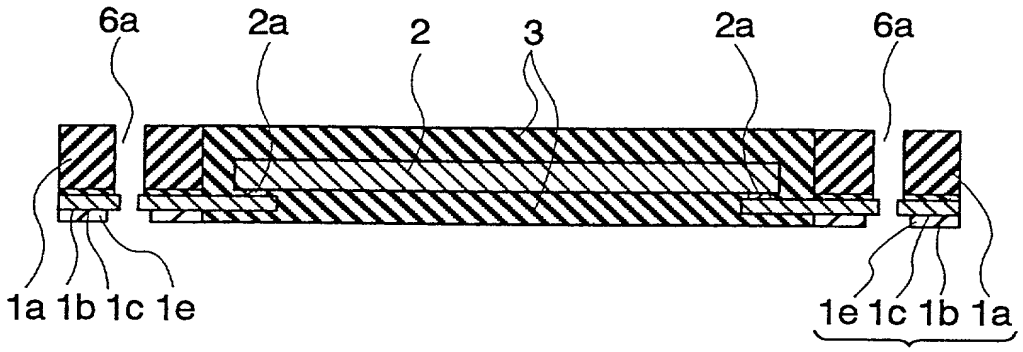


FIG. 21

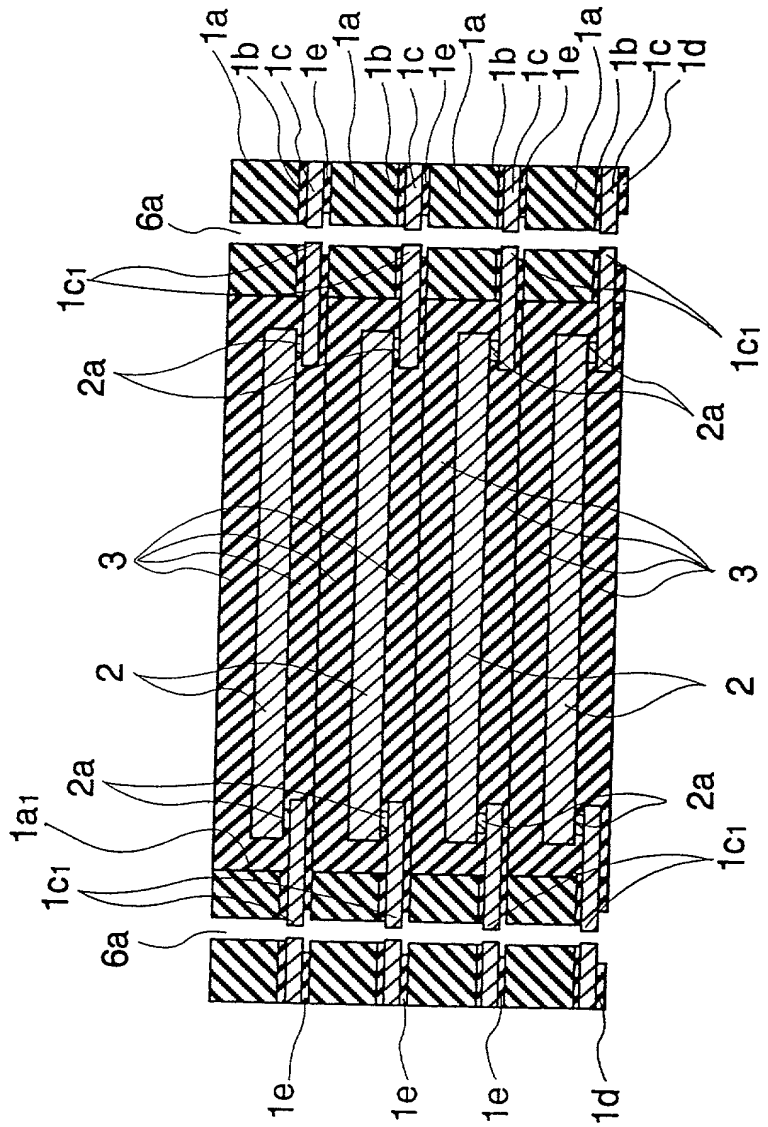


FIG. 22

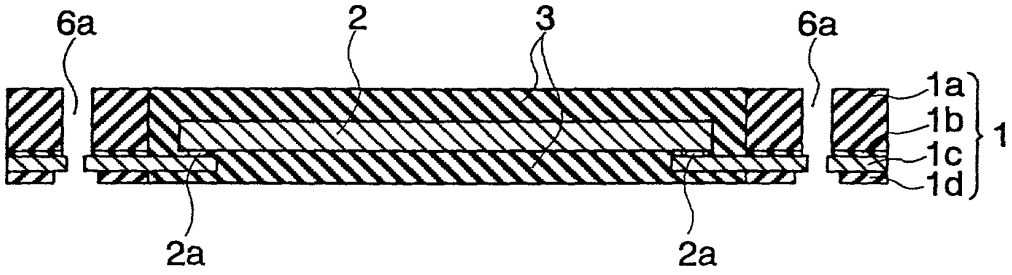


FIG. 23

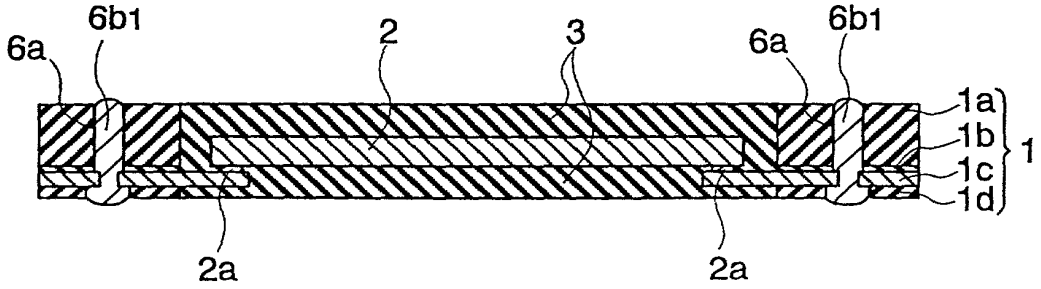


FIG. 24

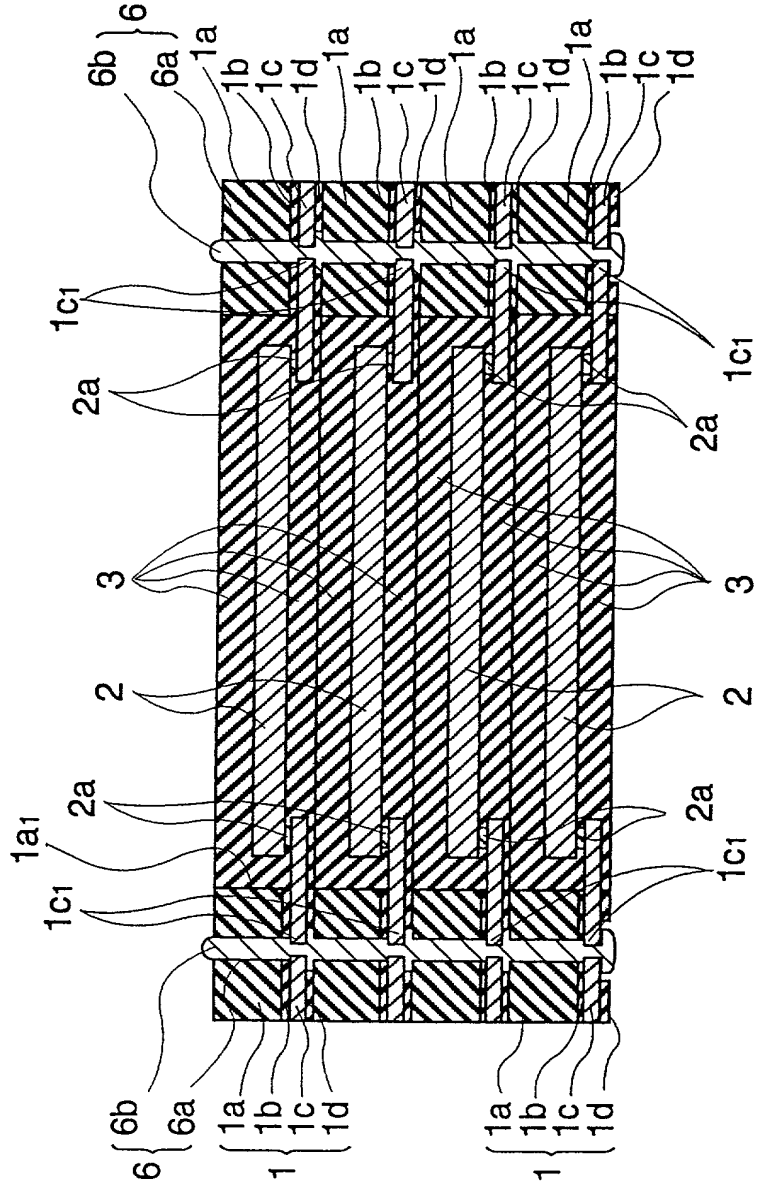


FIG. 25

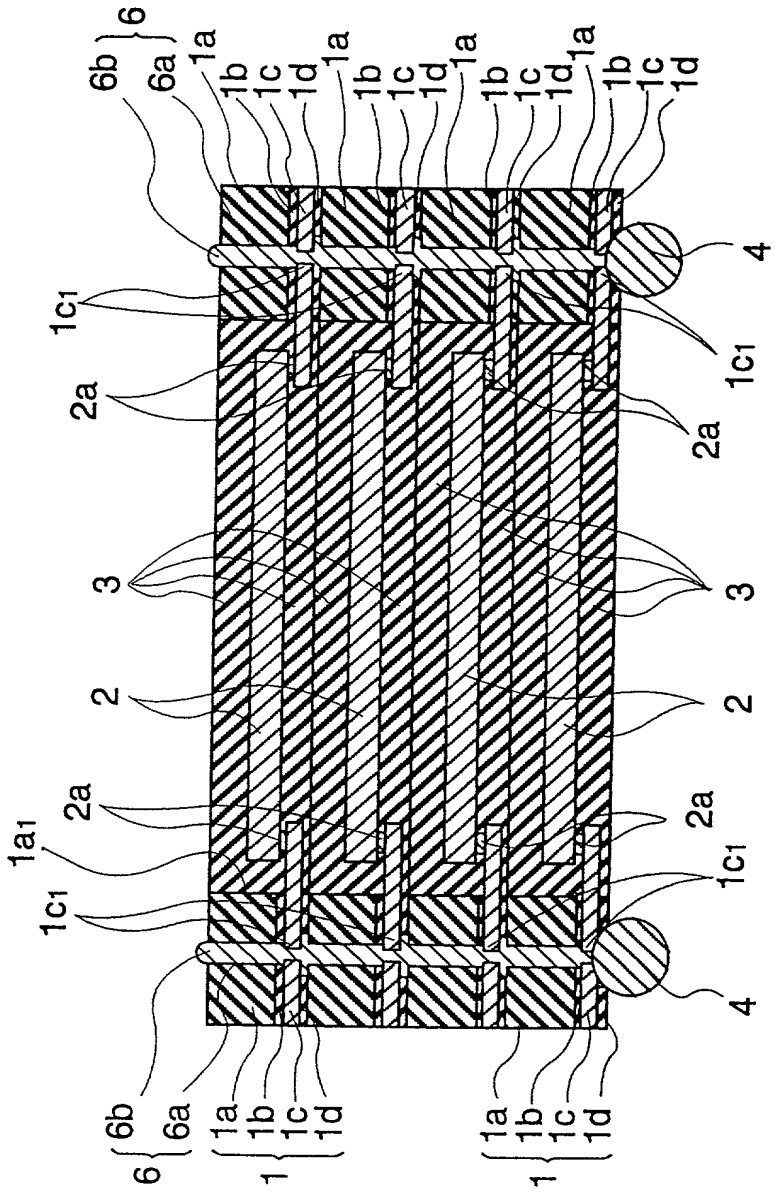


FIG. 26

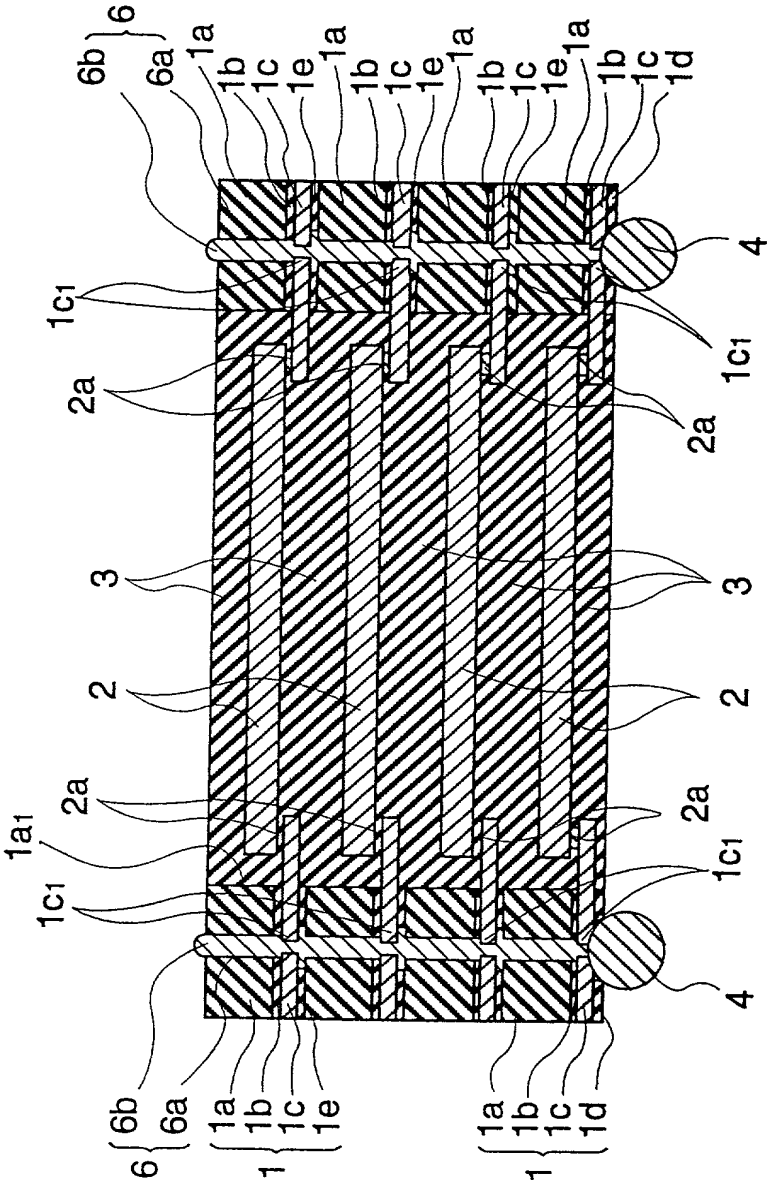
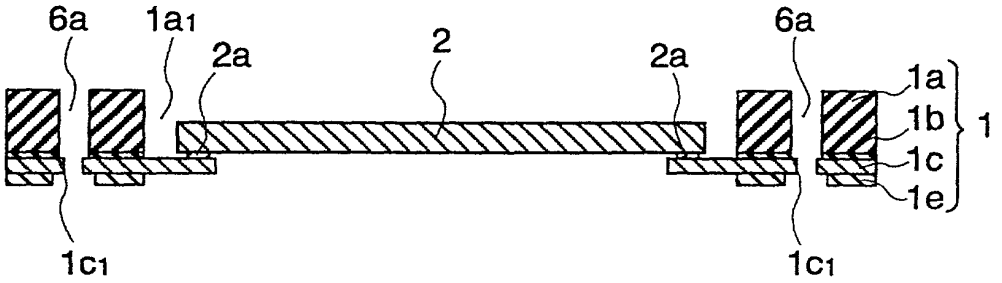


FIG. 27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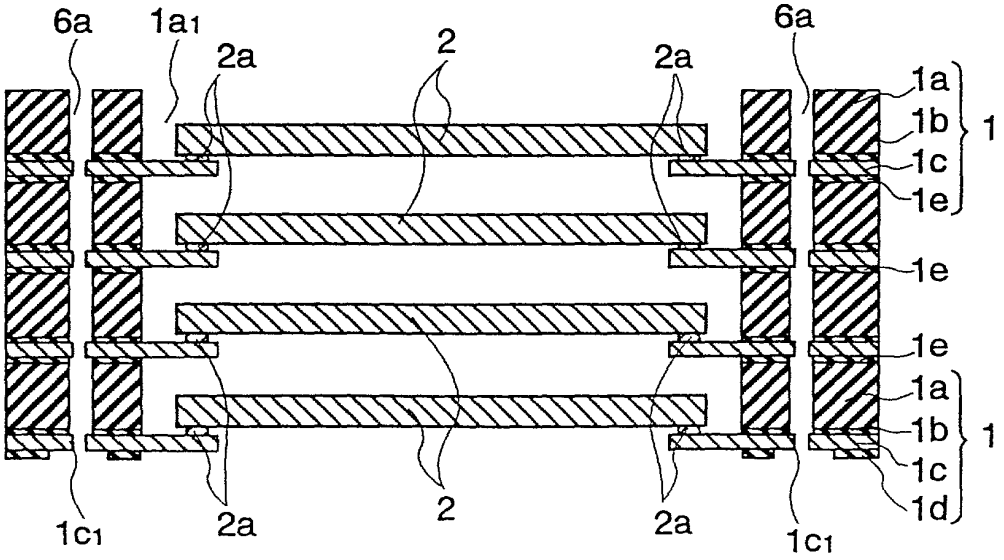
2a
2
2a
6a
1a
1b
1c
1e
1
1c1
1c1

FIG. 28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1a1
2a
2
2a
6a
1a
1b
1c
1e
1
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1e
1a
1b
1c
1d
1
1c1
2a
2
2a
1c1

FIG. 29

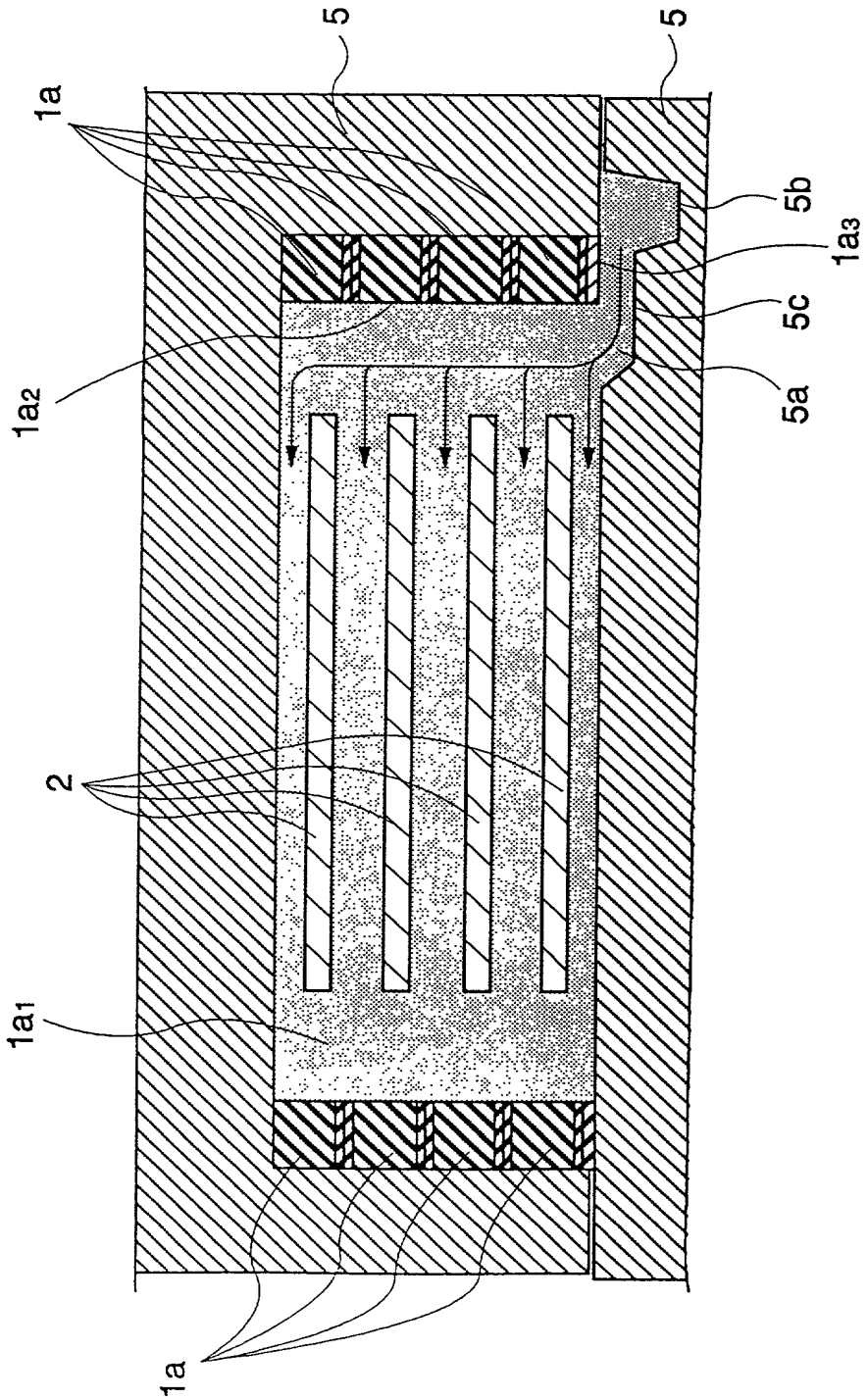


FIG. 30

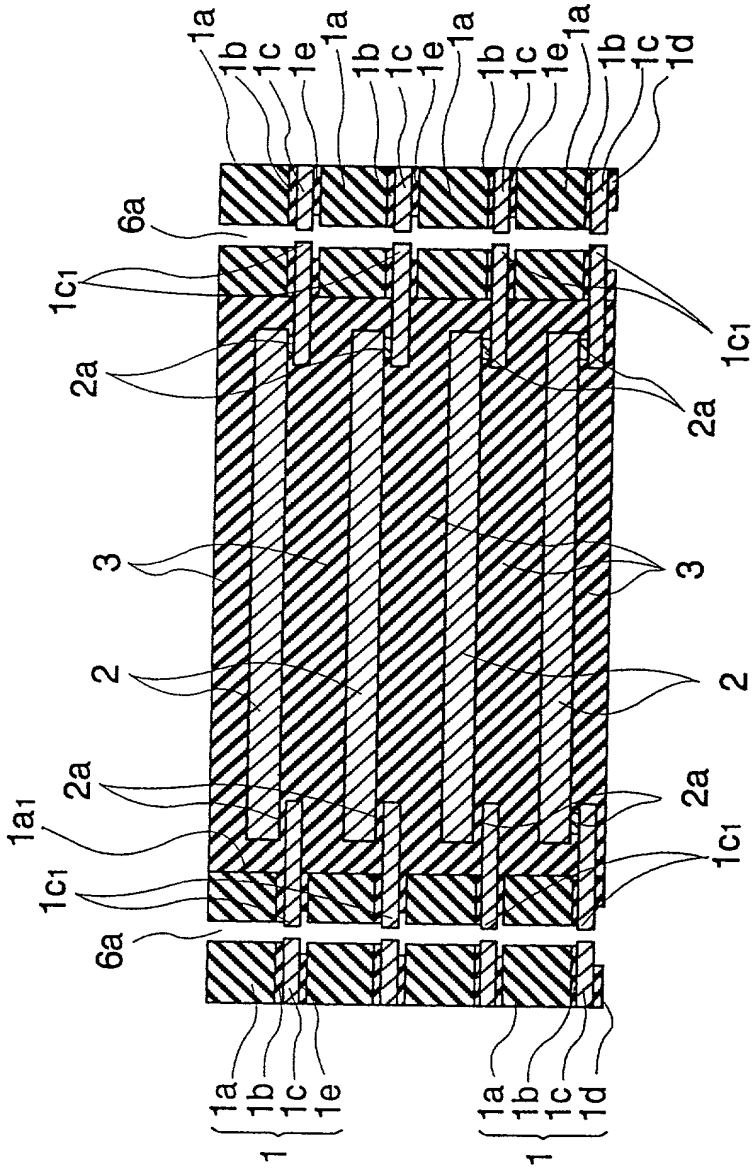


FIG. 31

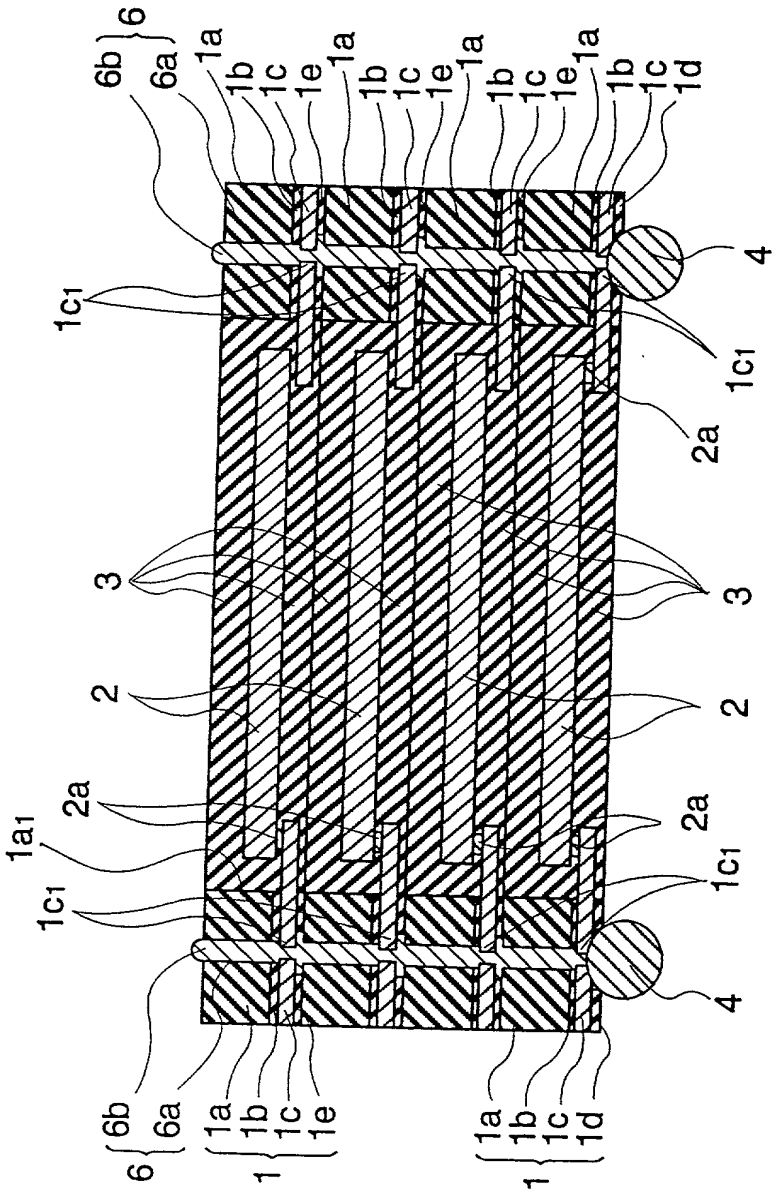


FIG. 32

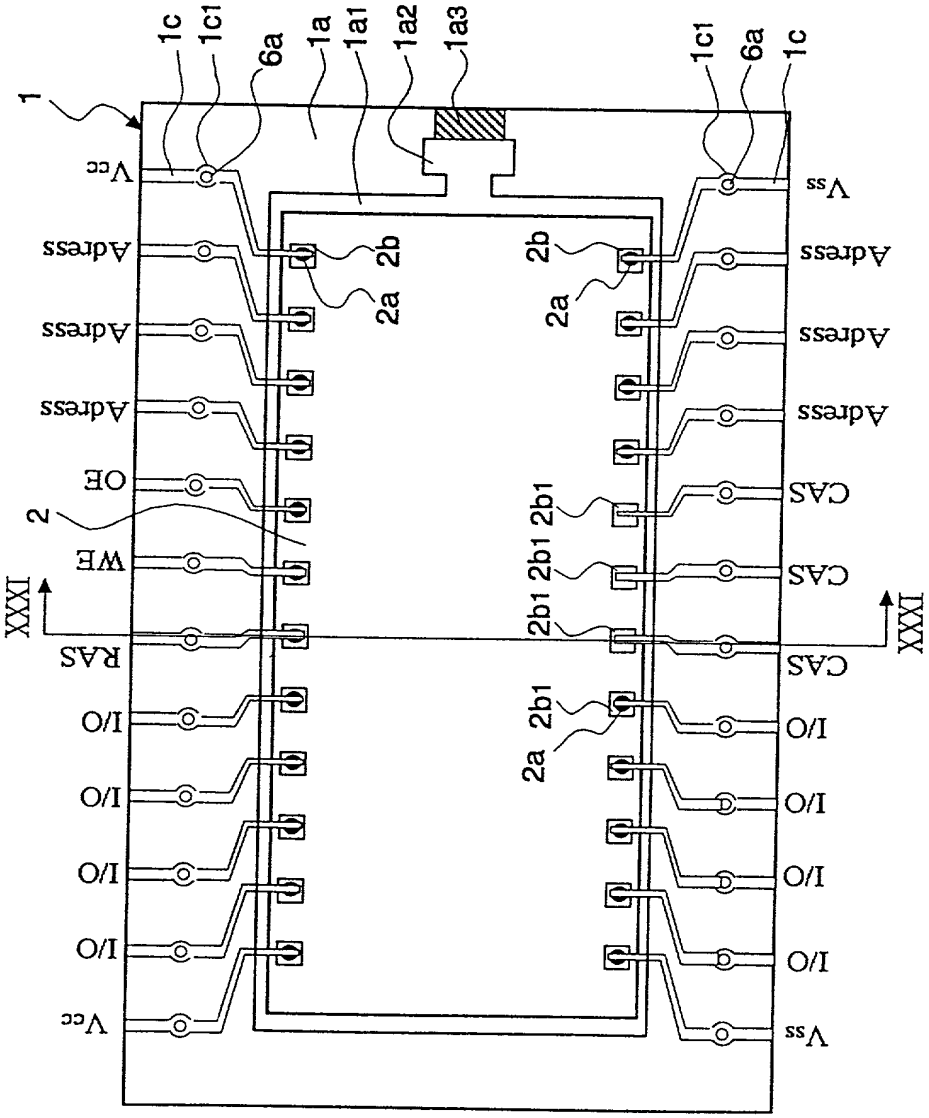

1
1c
1c1
6a
1a
1a1
1a2
1a3
Vcc
Address
OE
2
WE
XXX
RAS
I/O
2b
2a
2b1
CAS
Vss

FIG. 33

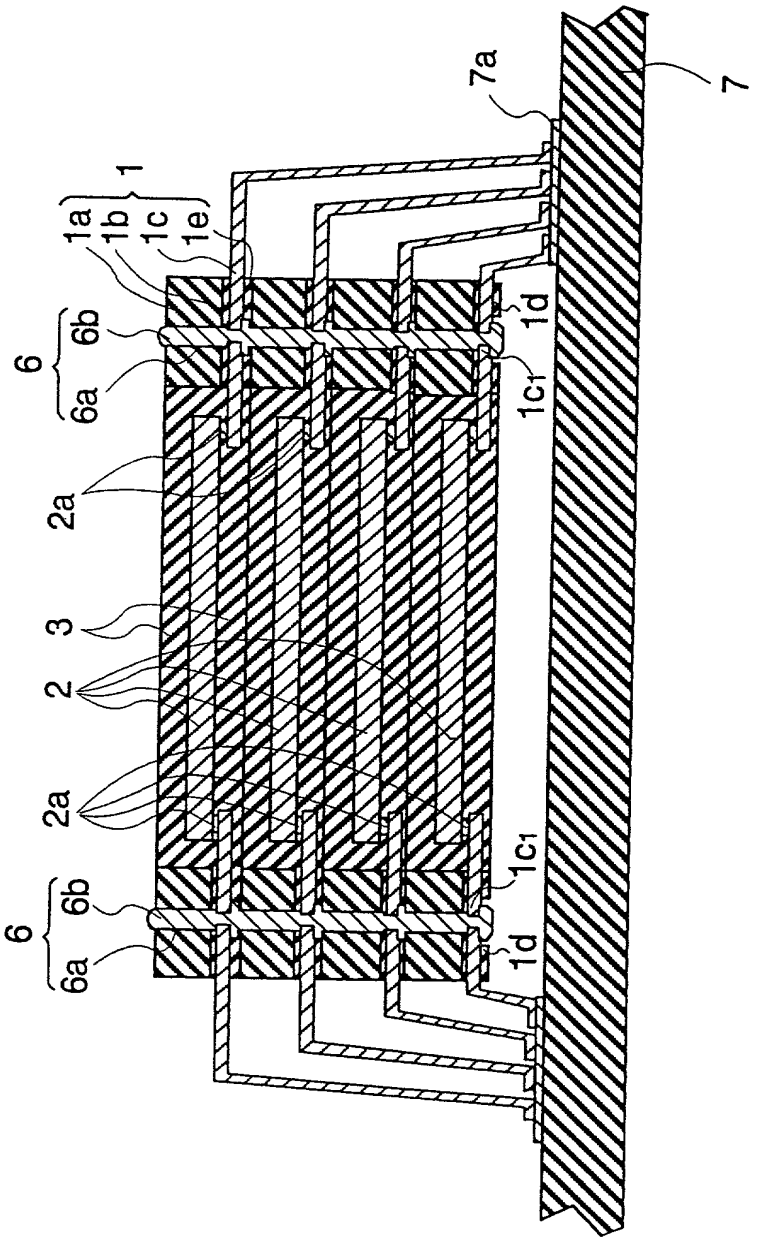


FIG. 34

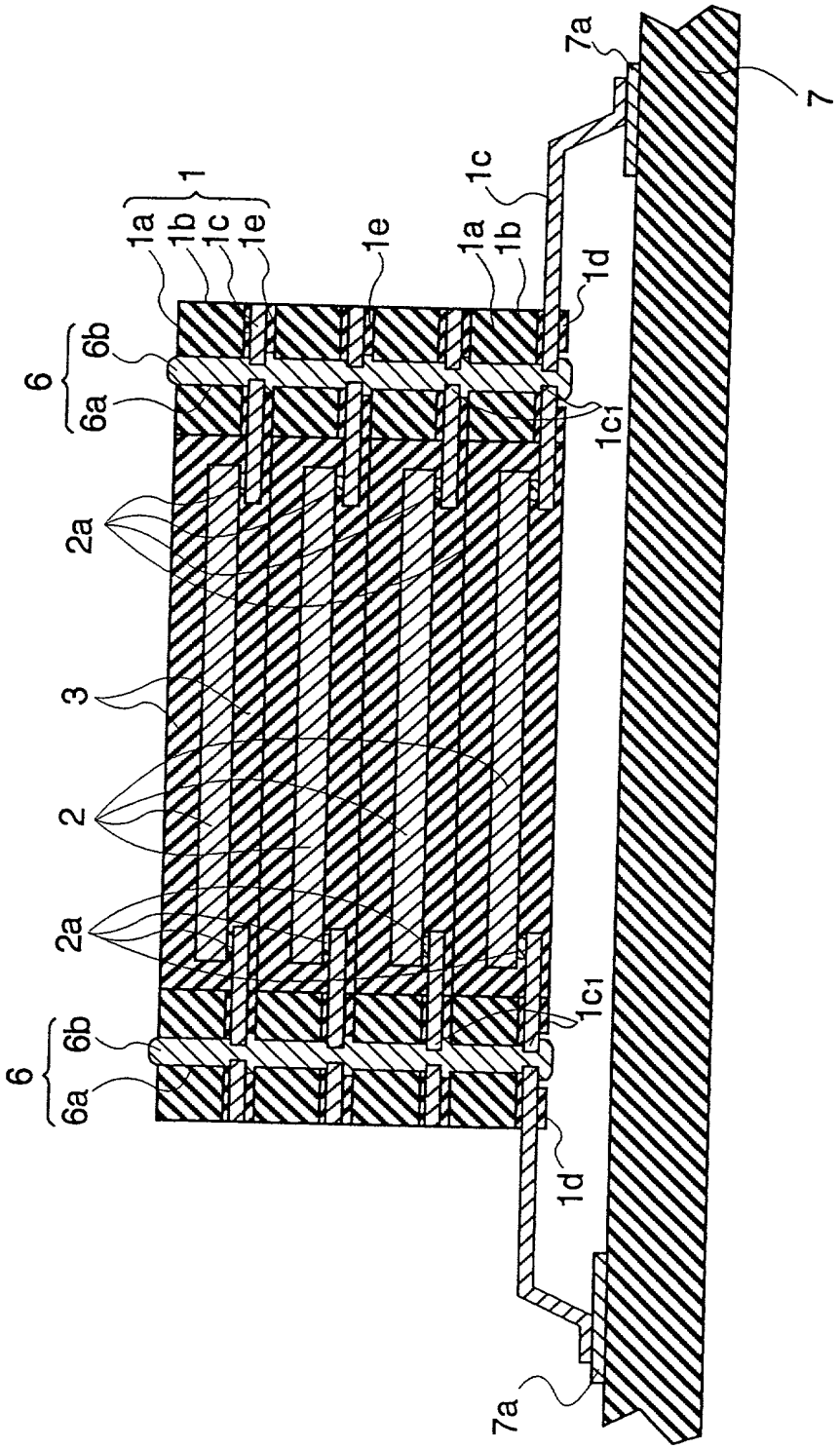


FIG. 35

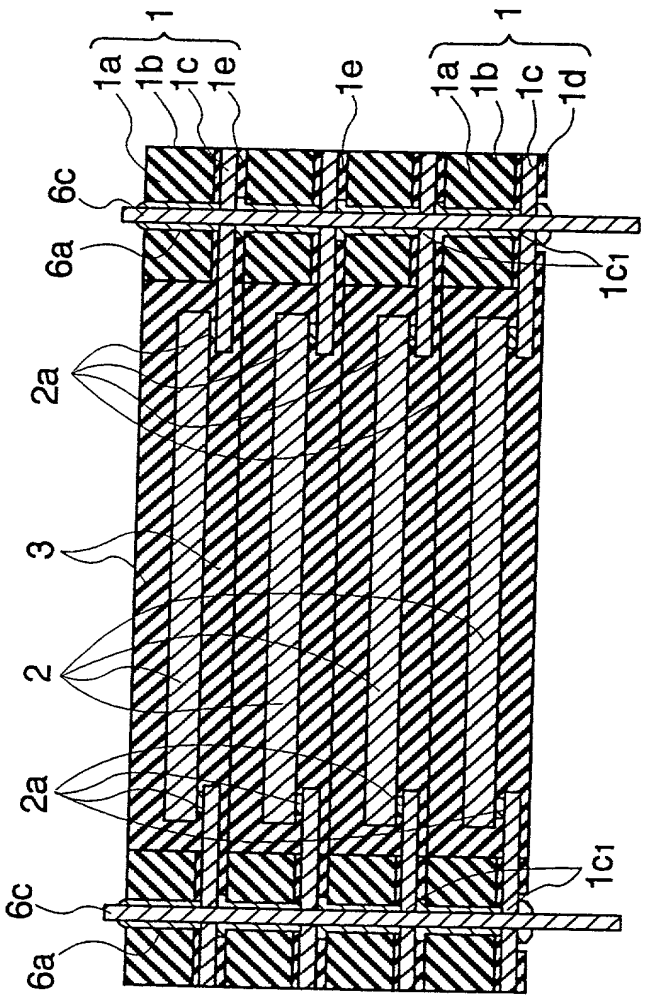


FIG. 36

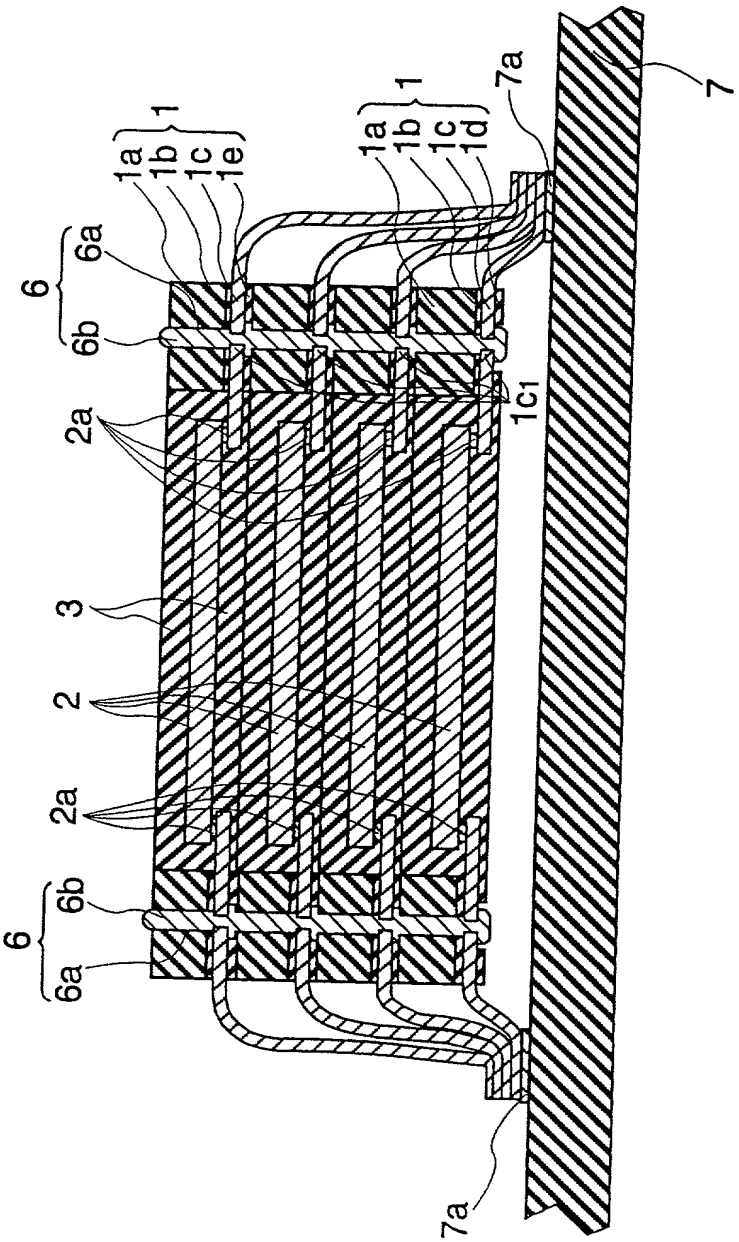


FIG. 37

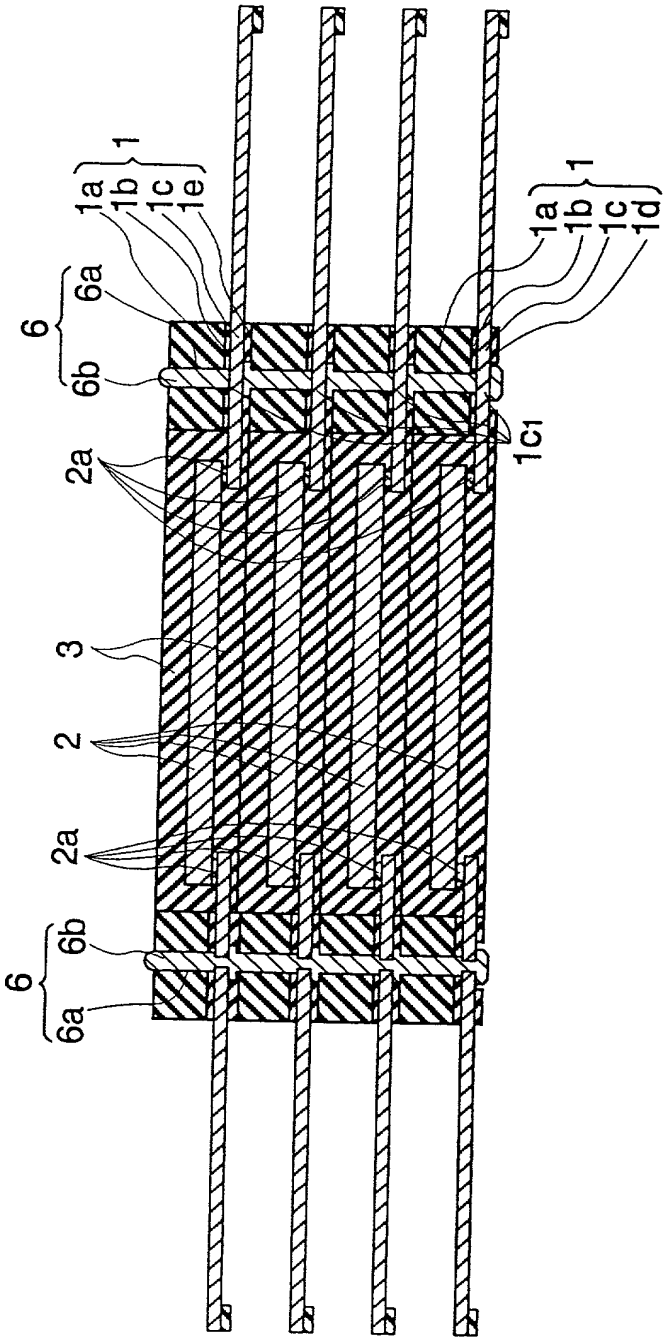


FIG. 38

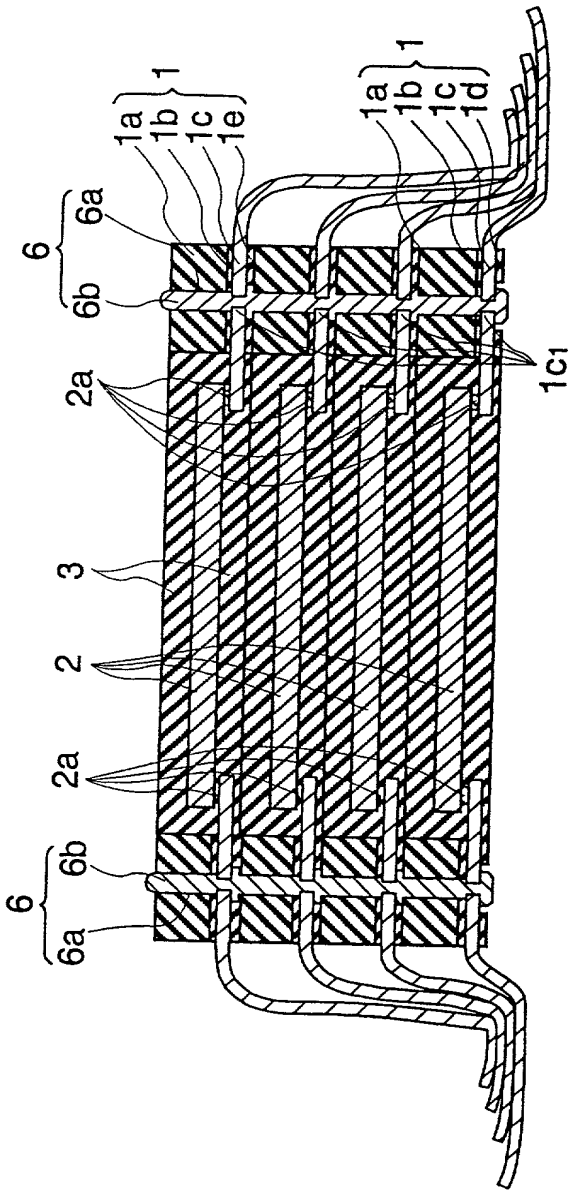


FIG. 39

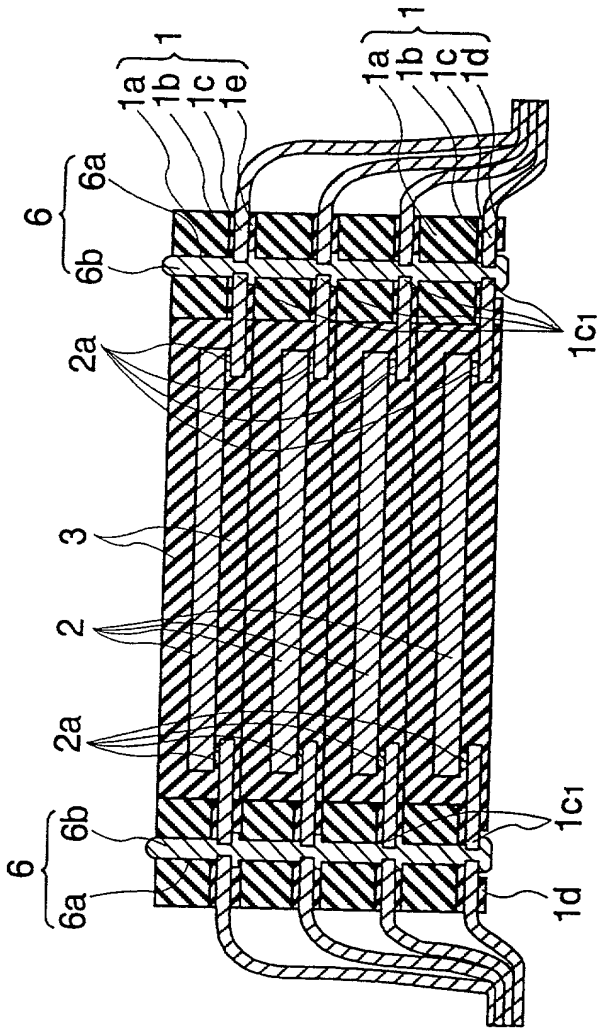


FIG. 40

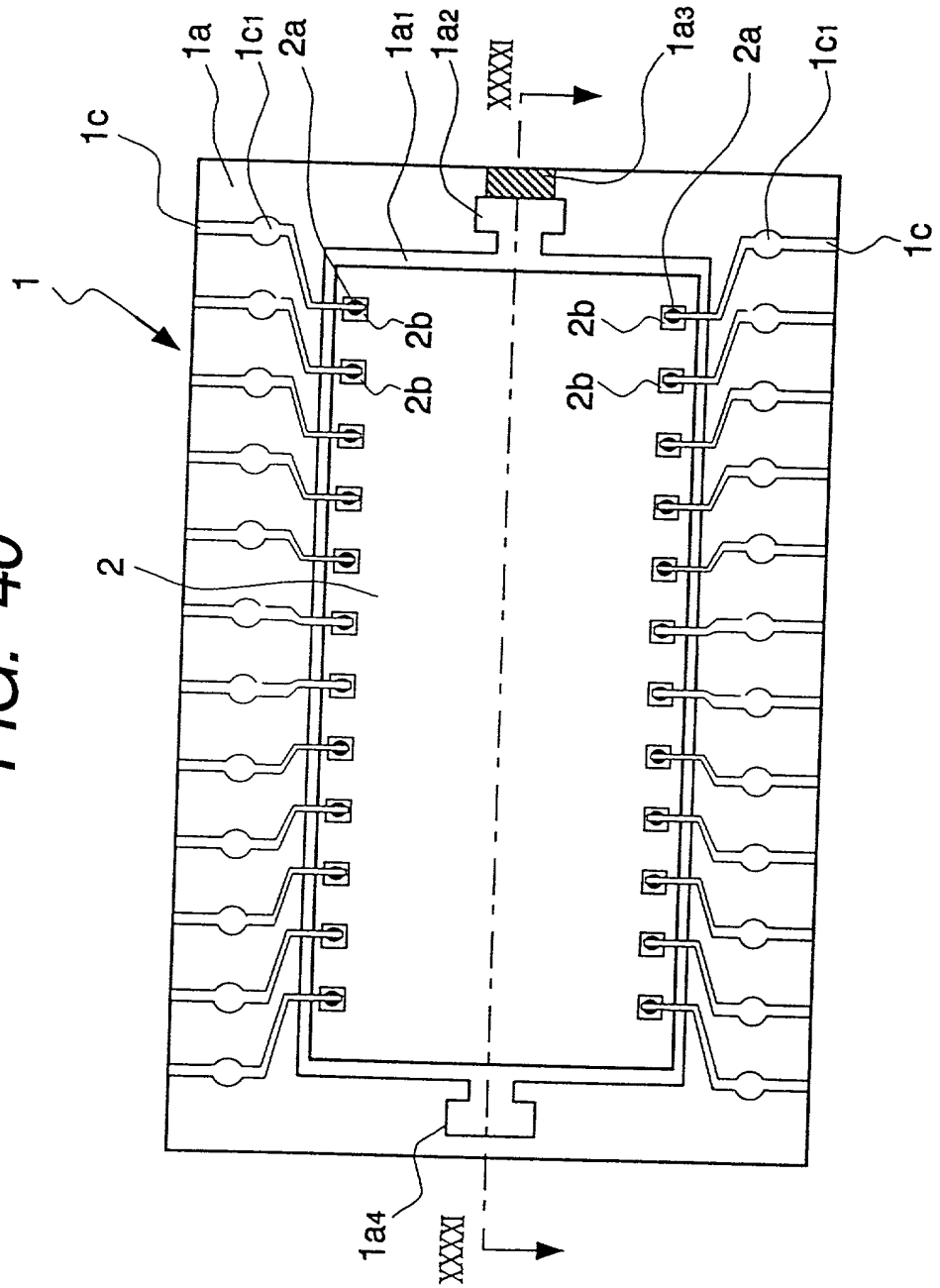
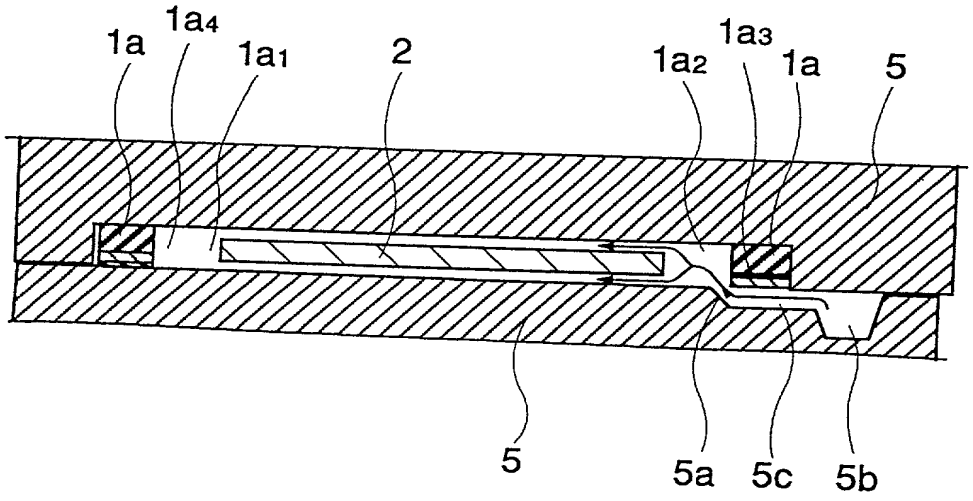


FIG. 41



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

the specification of which (check one) ☐ is attached hereto.

☒ was filed on May 20, 1999

as Application Serial No. _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

(Continued on Page 2)

I hereby appoint as principal attorneys; Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; Stanley A. Wal, Reg. No. 26,432; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621 to prosecute and transact all business connected with this application and any related United States application and international applications. Please direct all communications to the following address:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(Full Name) (Signature)

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Residence _____ Citizenship _____

Post Office Address _____

Date _____ Inventor _____

Residence _____ Citizenship _____

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Date _____ Inventor _____

Residence _____ Citizenship _____

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Date _____ Inventor _____

Residence _____ Citizenship _____

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Date _____ Inventor _____

Residence _____ Citizenship _____

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Filing Date	May 20, 1999
First Named Inventor	Kunihiro TSUBOSAKI
Group Art Unit	
Examiner Name	
Attorney Docket Number	501.37120X00

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